

SIMPLIS does not allow the multiplication or division of two (or more) dynamically-varying waveforms.

B1 1 2 V=V(4,8)*V(5,3)*15m is not allowed with Simplis

Instead, you must resort to logarithmic expressions to perform these operations:

Decimal base

$$\log_{10}(a \cdot b) = \log_{10} a + \log_{10} b$$

$$10^{(\log_{10} a + \log_{10} b)} = a \cdot b$$

e base

$$\ln(a \cdot b) = \ln a + \ln b$$

$$e^{(\ln a + \ln b)} = a \cdot b$$

For a division:

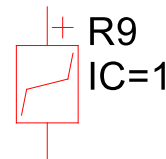
$$\log_{10}\left(\frac{a}{b}\right) = \log_{10} a - \log_{10} b$$

$$10^{(\log_{10} a - \log_{10} b)} = \frac{a}{b}$$

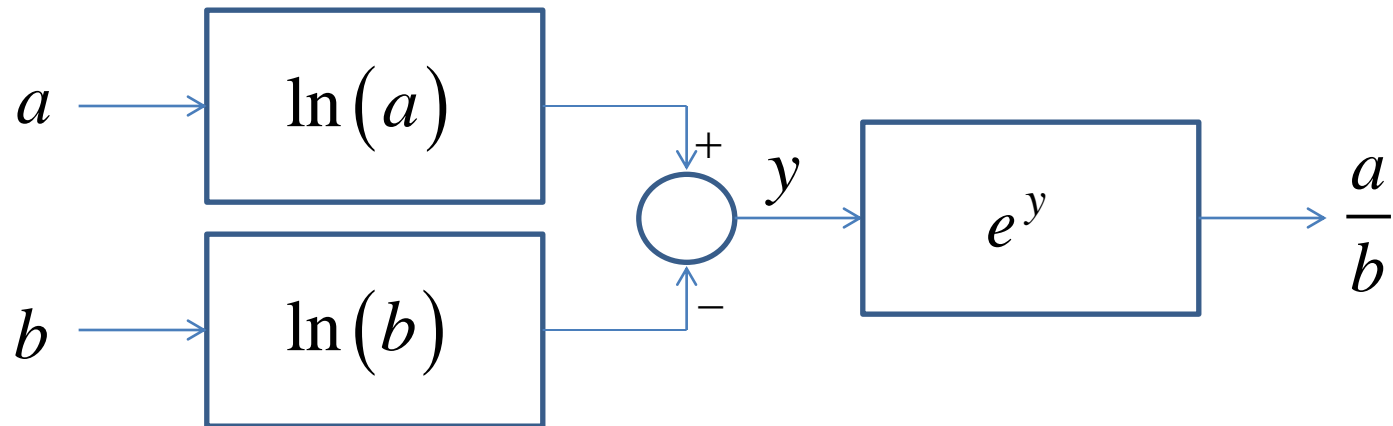
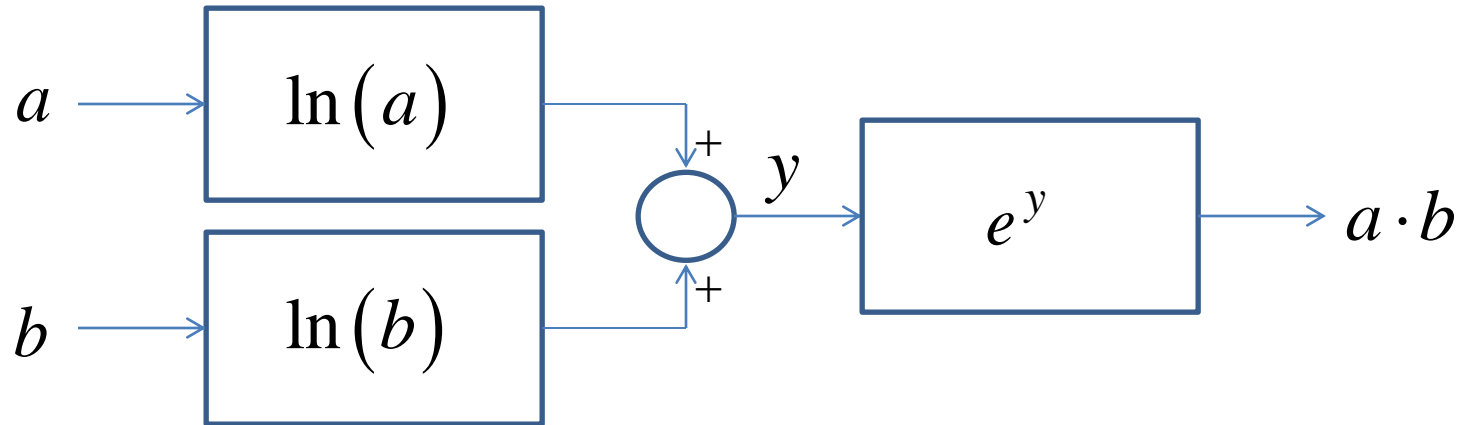
$$\ln\left(\frac{a}{b}\right) = \ln a - \ln b$$

$$e^{(\ln a - \ln b)} = \frac{a}{b}$$

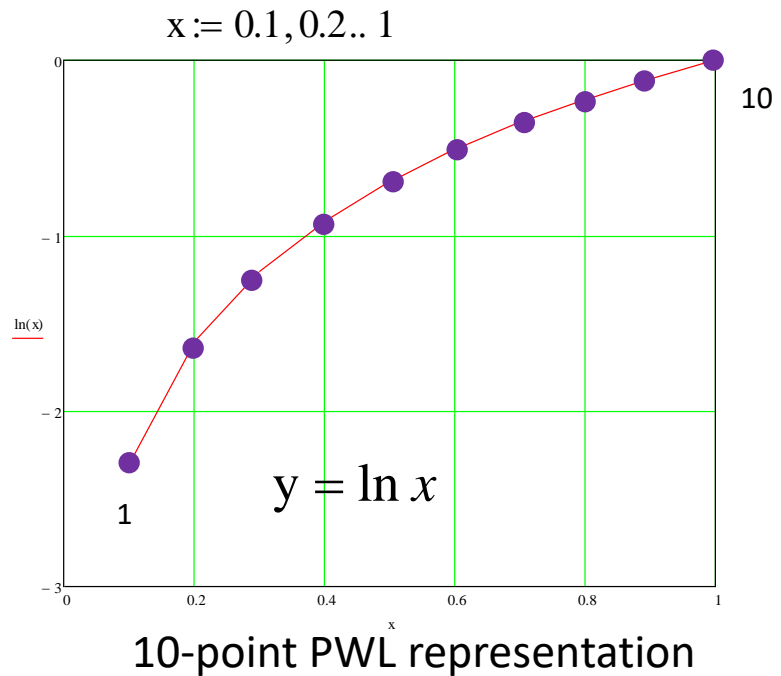
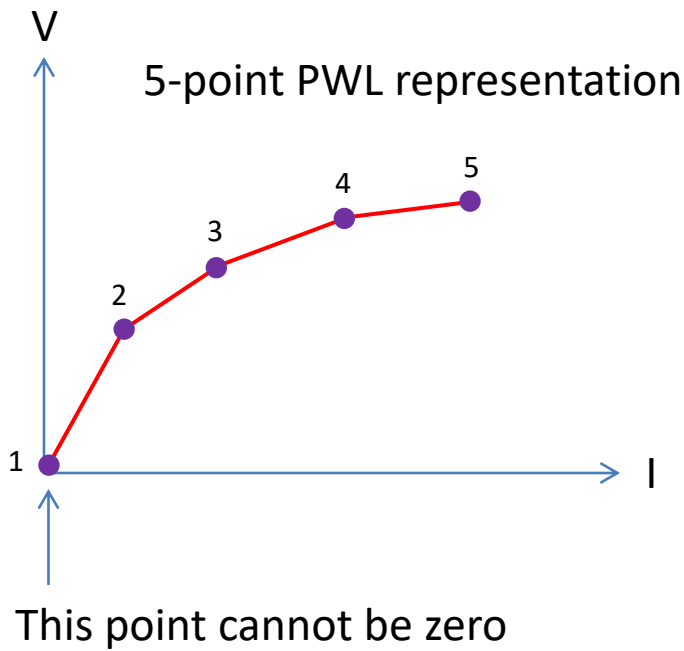
SIMPLIS offers a way to create functions in a piece-wise-linear way via a PWL component, the VPWL or IPWL resistor:



You will have to take the logarithm of the considered variables and sum/subtract them before taking the exponential of the result.



You will have to know the range within which a and b vary but also the range within which y will vary. This is important to make sure the variation remains within the adopted data points.

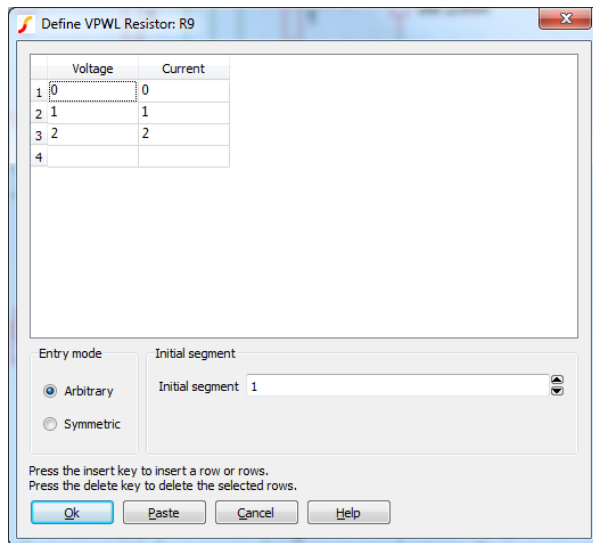


The best tool is actually Excel since the generated values will be copied/pasted into the selected SIMPLIS V or IPWL element

	Input			Output			
	A	B	C	D	E	F	G
1		x	Ln(x)		x	exp(x)	
2		1.00E-01	-2.30259		-2.30259	0.1	
3		2.00E-01	-1.60944		-1.60944	0.2	
4		3.00E-01	-1.20397		-1.20397	0.3	
5		4.00E-01	-0.91629		-0.91629	0.4	
6		5.00E-01	-0.69315		-0.69315	0.5	
7		6.00E-01	-0.51083		-0.51083	0.6	
8		7.00E-01	-0.35667		-0.35667	0.7	
9		8.00E-01	-0.22314		-0.22314	0.8	
10		9.00E-01	-0.10536		-0.10536	0.9	
11		1.00E+00	-1.1E-16		-1.1E-16	1	
12							

The range is given by the input signals while the number of points depends on the expected precision in the calculation. Assuming a 0-1 V input range with crude variations in 150 or 200 mV steps. In this case, perhaps 10-20 points will suffice to map the input signal into the lookup table. If the input signal is going through small increments, increase the number of point with 10-20-mV steps.

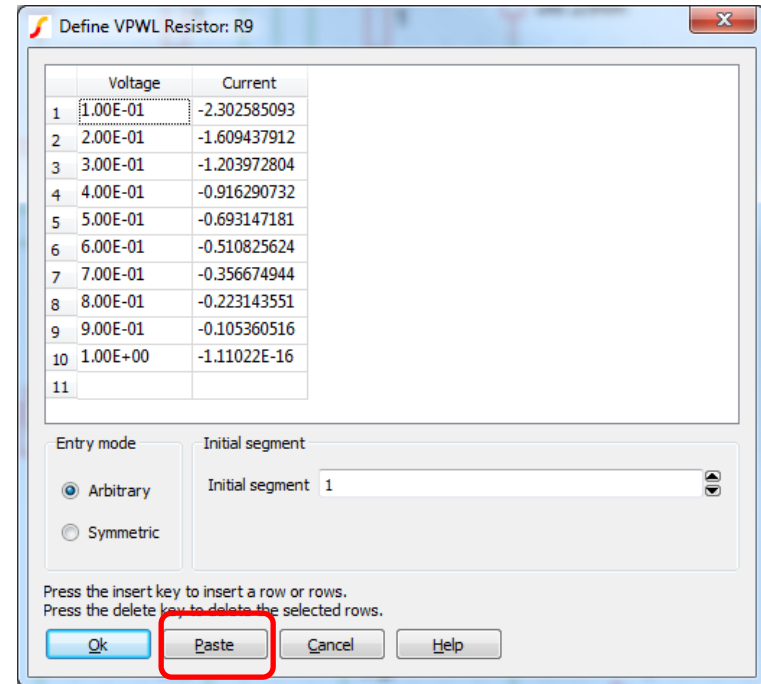
Double-click on the newly-placed VPWL element:



Select data in Excel - Copy

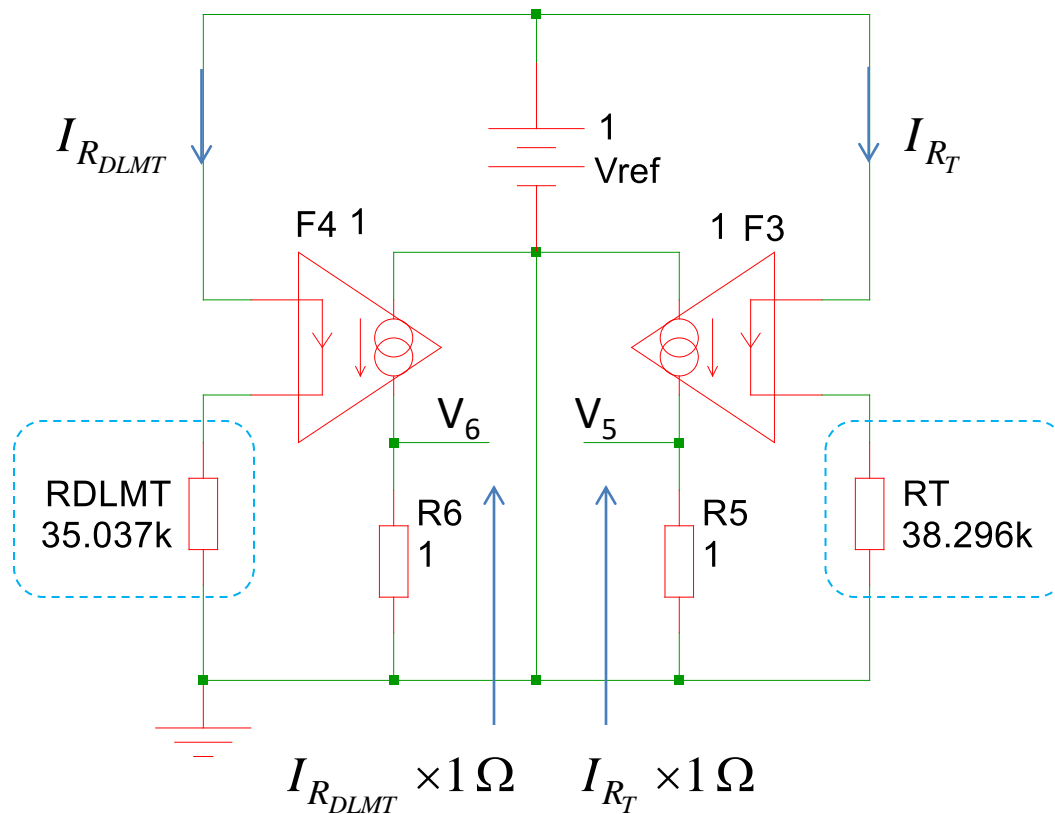
x	Ln(x)
1.00E-01	-2.30259
2.00E-01	-1.60944
3.00E-01	-1.20397
4.00E-01	-0.91629
5.00E-01	-0.69315
6.00E-01	-0.51083
7.00E-01	-0.35667
8.00E-01	-0.22314
9.00E-01	-0.10536
1.00E+00	-1.1E-16

Press Paste to paste the data into the array



You want to multiply two currents together:

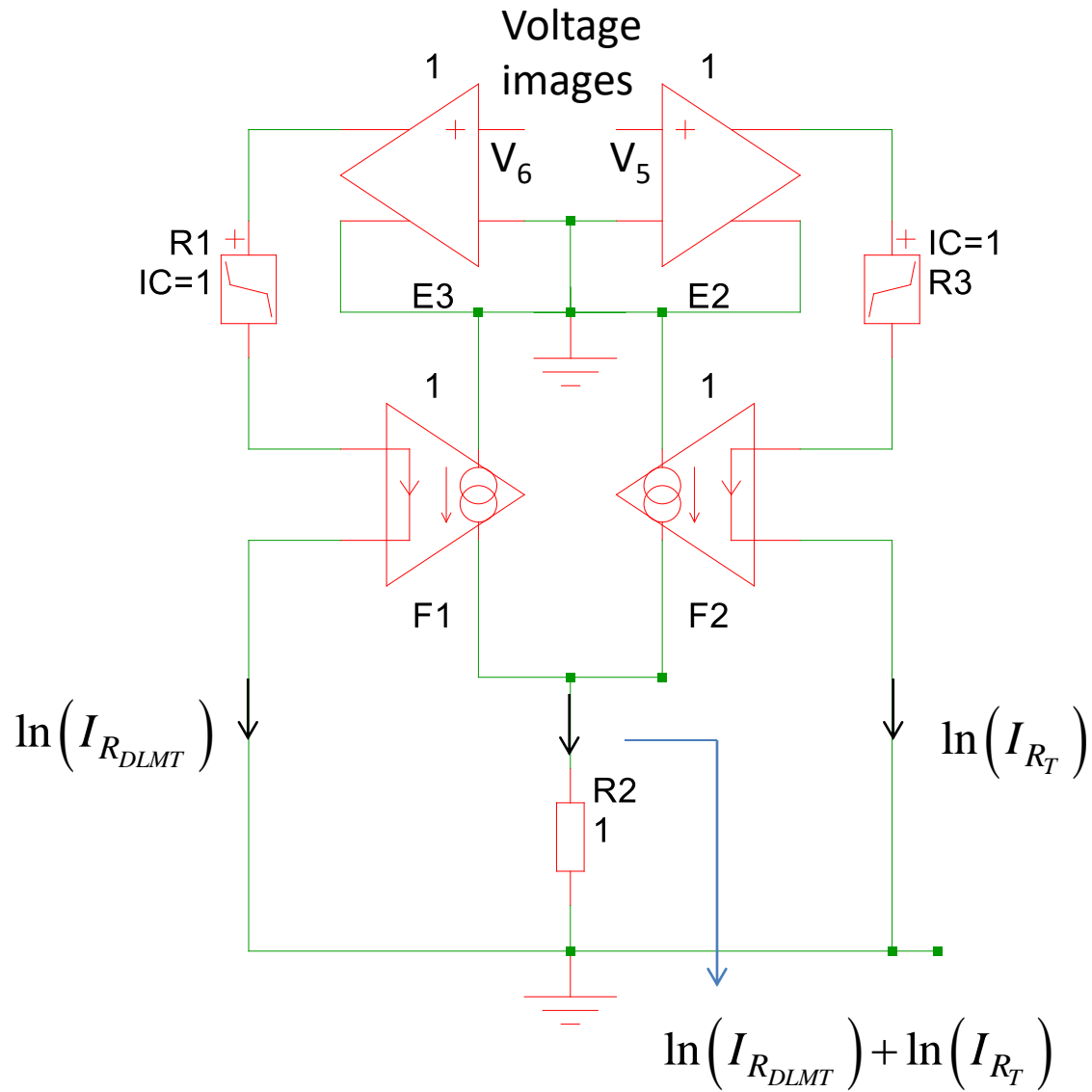
1. Mirror current variables via a F source and transform them into a voltage



These resistors program the chip currents by absorbing current from the 1-V bias.

Voltage images of the currents circulating in RDLMT and RT

2. Take the natural logarithm of the buffered voltages



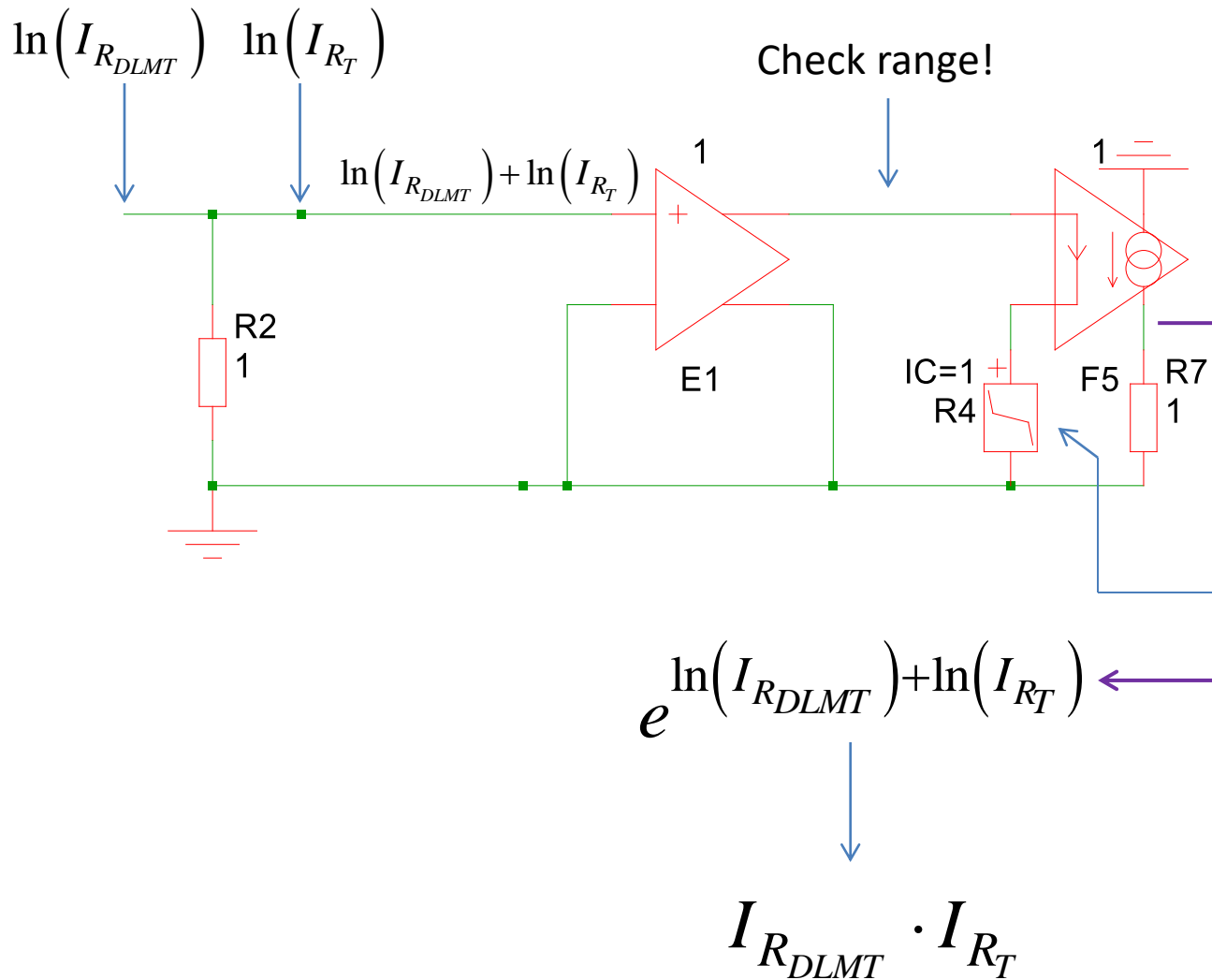
The biasing voltage for the resistances is 1 V. Typical values for the resistances range from 10 k Ω to 70 k Ω . As such, the current may vary from 100 μ A down to 15 μ A. I've built a VPWL following the below list: 1 μ V to 100 μ V by 1 μ V steps (100 points).

	Voltage	Current
1	1.00E-06	-13.81551056
2	2.00E-06	-13.12236338
3	3.00E-06	-12.71689827
4	4.00E-06	-12.4292162
5	5.00E-06	-12.20607265
6	6.00E-06	-12.02375109
7	7.00E-06	-11.86960041
8	8.00E-06	-11.73606902
9	9.00E-06	-11.61828598
10	1.00E-05	-11.51292546
11	1.10E-05	-11.41761529
12	1.20E-05	-11.33060391
13	1.30E-05	-11.2505612
14	1.40E-05	-11.17645323
15	1.50E-05	-11.10746036
16	1.60E-05	-11.04292184
17	1.70E-05	-10.98229721
18	1.80E-05	-10.9251388
19	1.90E-05	-10.87107158
20	2.00E-05	-10.81977828
21	2.10E-05	-10.77098812
22	2.20E-05	-10.7244681
23	2.30E-05	-10.68001634
24	2.40E-05	-10.63745673

R_1
 R_3

You see in the right side the resulting current which ranges from -13.8 A to -9.2 A. Summing these values implies a total current representative of the two currents ranging from -30 A to -17.6 A.

Now that we have the sum of the natural logarithms, we need to take the exponential of the buffered result to obtain the wanted multiplication.



Check range!

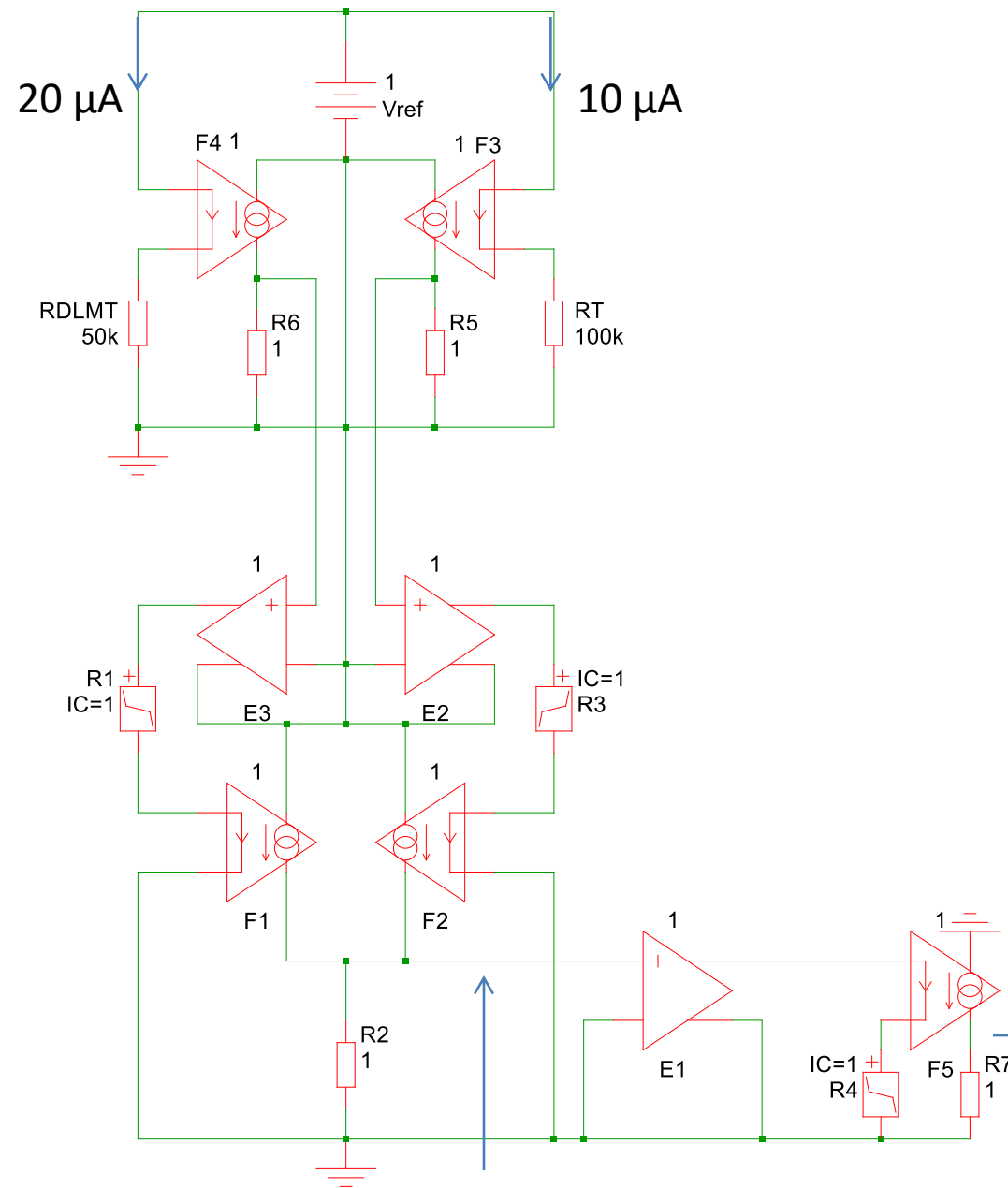
Define VPWL Resistor: R4

	Voltage	Current
1	-30	9.35762E-14
2	-29.95	9.8374E-14
3	-29.9	1.03418E-13
4	-29.85	1.0872E-13
5	-29.8	1.14294E-13
6	-29.75	1.20154E-13
7	-29.7	1.26315E-13
8	-29.65	1.32791E-13
9	-29.6	1.39599E-13
10	-29.55	1.46757E-13
11	-29.5	1.54281E-13
12	-29.45	1.62191E-13
13	-29.4	1.70507E-13
14	-29.35	1.79249E-13
15	-29.3	1.88439E-13
16	-29.25	1.98101E-13
17	-29.2	2.08258E-13
18	-29.15	2.18935E-13
19	-29.1	2.3016E-13
20	-29.05	2.41961E-13
21	-29	2.54367E-13
22	-28.95	2.67408E-13
23	-28.9	2.81119E-13
24	-28.85	2.95532E-13
25	-28.8	3.10685E-13

Entry mode Initial segment

Range is likely to be between -30 to -17 A, setting the VPWL limits.

-17.6

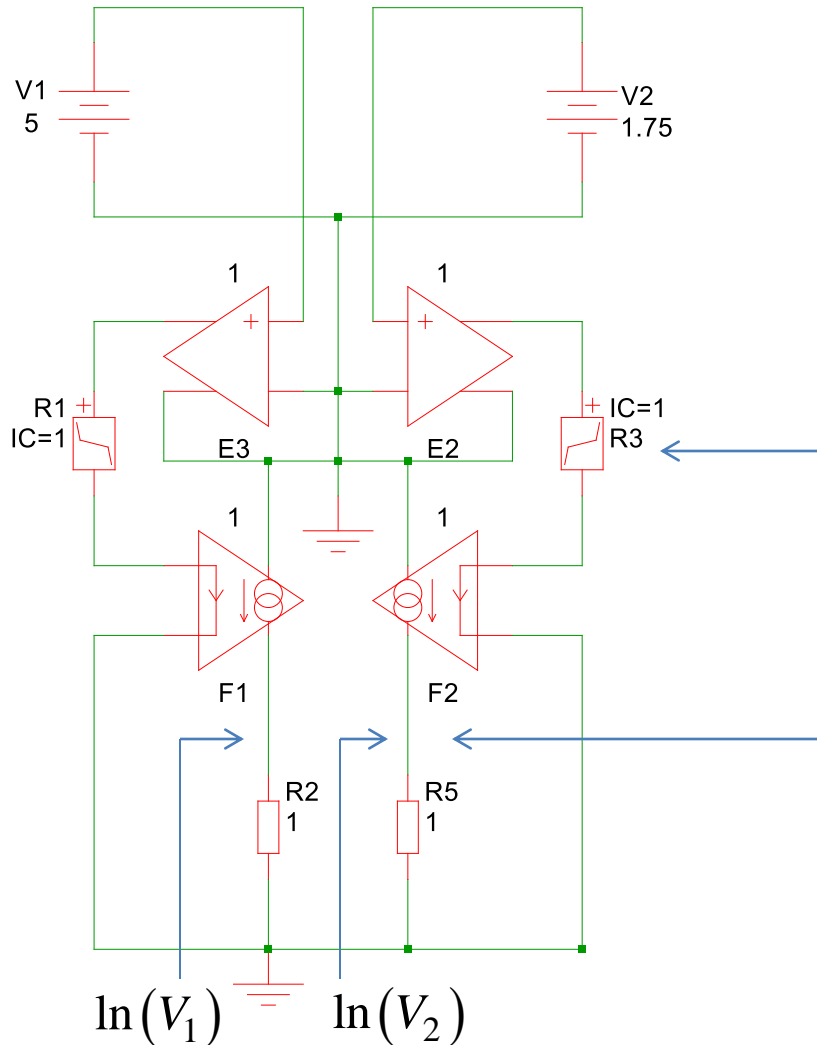


200.0566 pV
 $e^{-22.333} = 1.999 \times 10^{-10}$

$\ln(20 \cdot 10^{-6}) + \ln(10 \cdot 10^{-6}) = -22.333$

For a division, you need to reverse the sign when summing both logarithmic currents. Assume you want to divide V_1 by V_2 . Both voltages vary between 200 mV to 5 V in crude steps.

Ln function



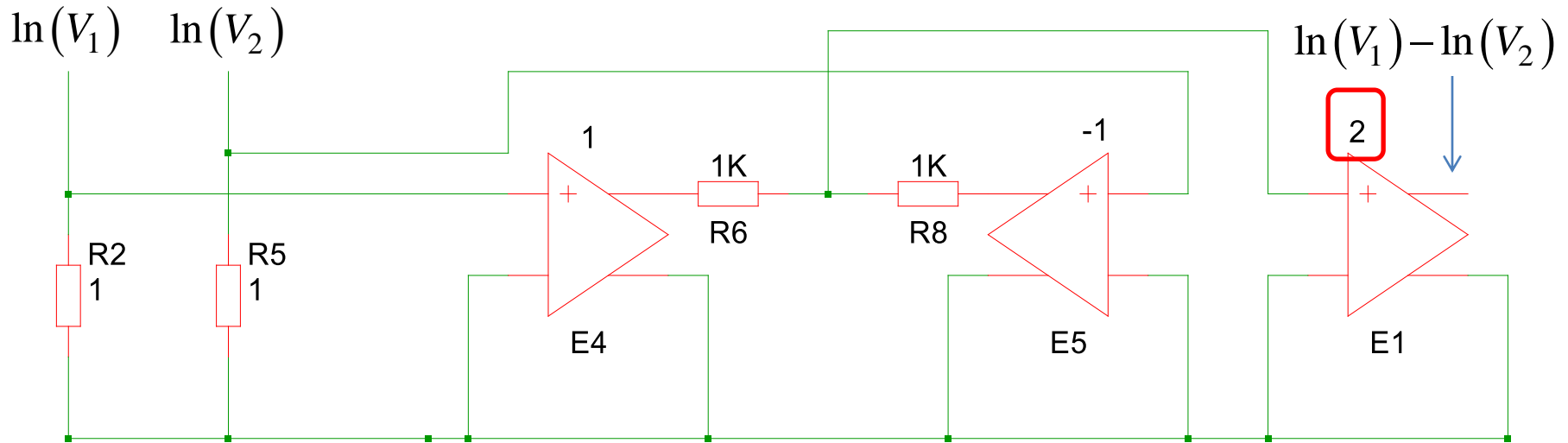
Define VPWL Resistor: R1

	Voltage	Current
1	2.00E-01	-1.609437912
2	8.00E-01	-0.223143551
3	1.40E+00	0.336472237
4	2.10E+00	0.741937345
5	2.60E+00	0.955511445
6	3.10E+00	1.131402111
7	3.60E+00	1.280933845
8	4.10E+00	1.410986974
9	4.60E+00	1.526056303
10	5.10E+00	1.62924054

Current (but voltage across the 1- Ω res) sets the range: -1.6 V to 1.7 V

Buffer the voltage inputs and transform into a currents flowing in the 1- Ω resistors

Then subtract the two voltage outputs. May ways to sum voltages, this one is one possibility.



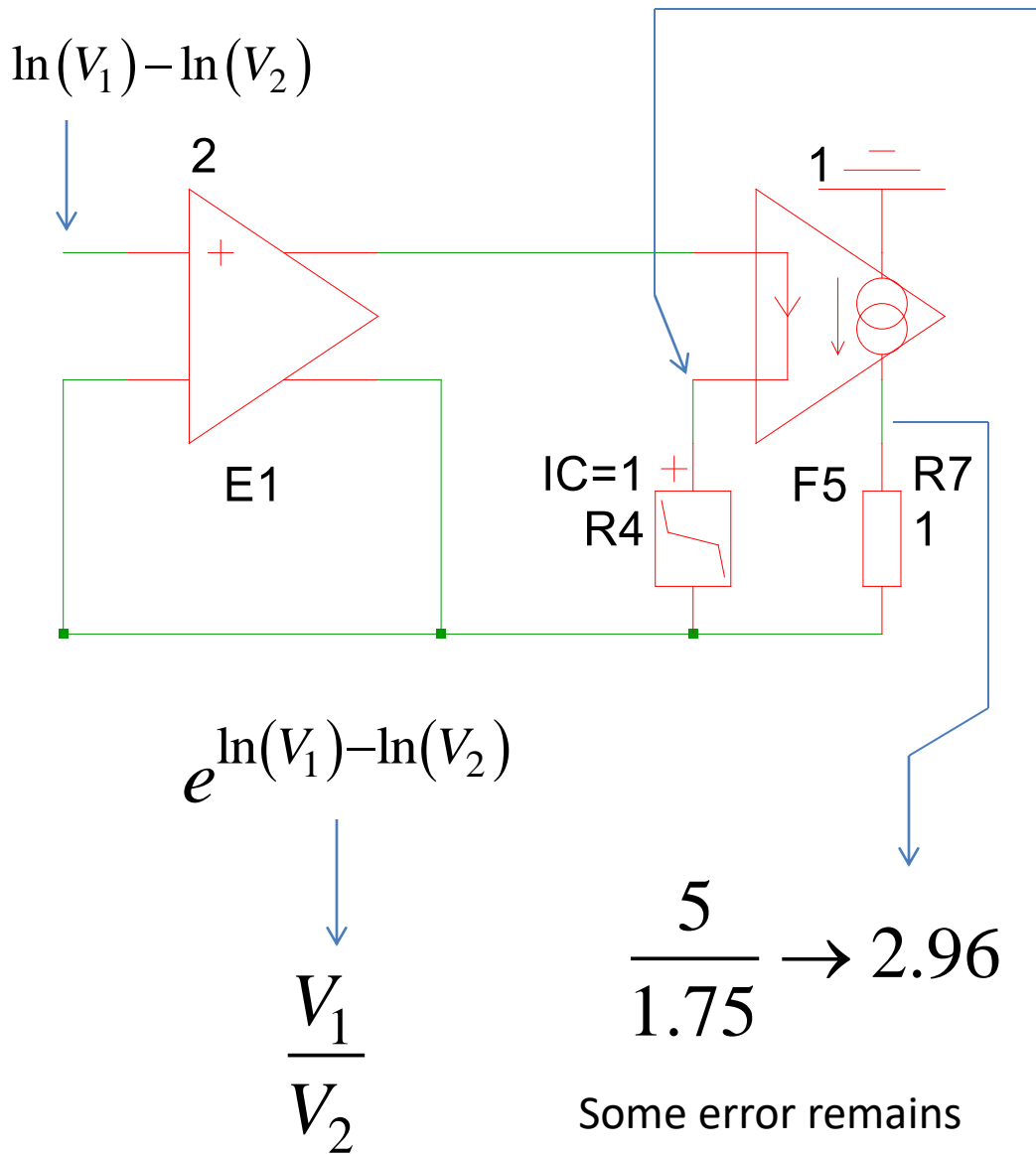
$$\ln(V_1) - \ln(V_2)$$

$$\ln(10m) - \ln(5) = -6$$

$$\ln(5) - \ln(0.01) = 6$$

range will be between - 6 to 6 V

We will now calculate the exponential of the subtracted voltages

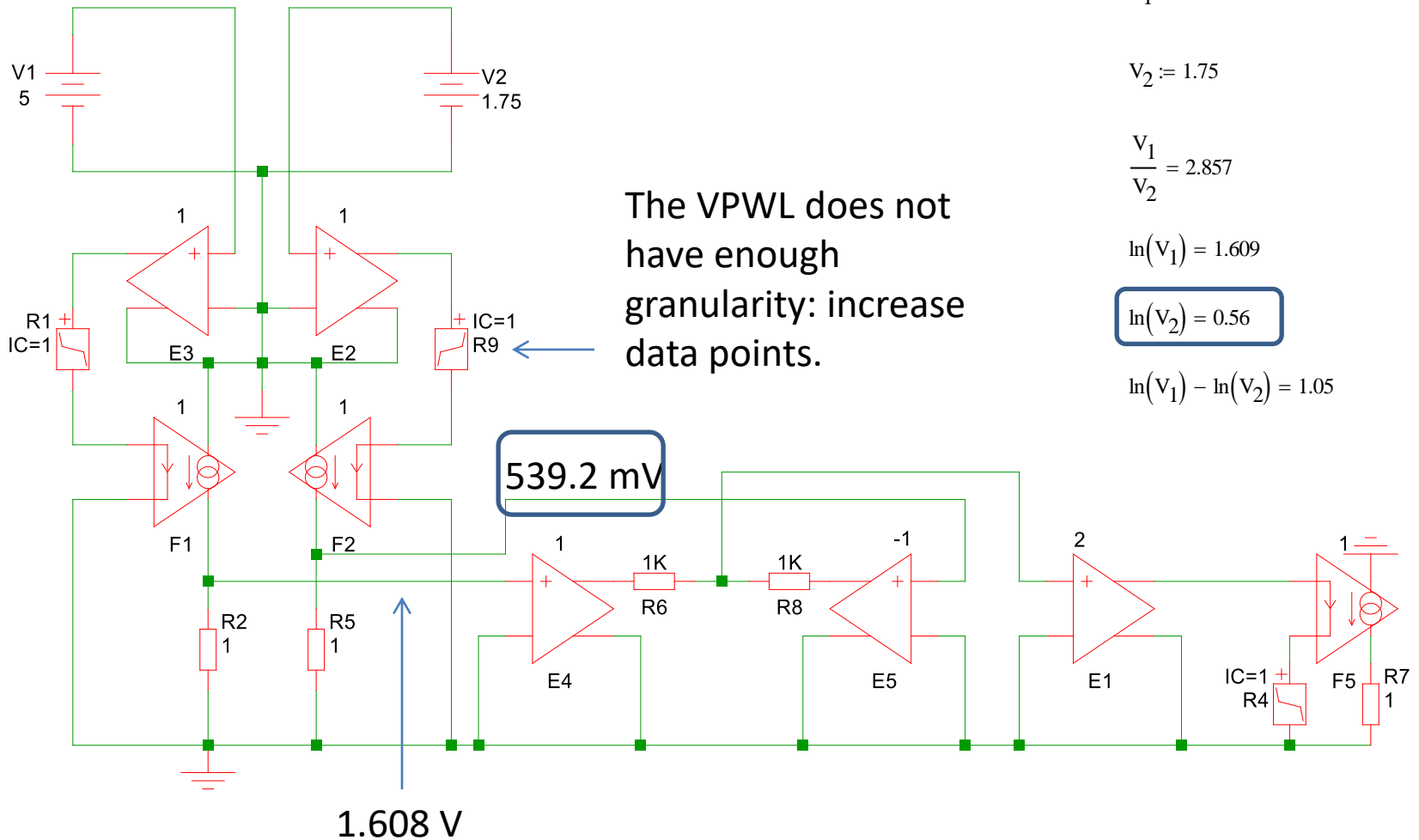


Define VPWL Resistor: R4

	Voltage	Current
1	-6	0.002478752
2	-5.5	0.004086771
3	-5	0.006737947
4	-4.5	0.011108997
5	-4	0.018315639
6	-3.5	0.030197383
7	-3	0.049787068
8	-2.5	0.082084999
9	-2	0.135335283
10	-1.5	0.22313016
11	-1	0.367879441
12	-0.5	0.60653066
13	0	1
14	0.5	1.648721271
15	1	2.718281828
16	1.5	4.48168907
17	2	7.389056099
18	2.5	12.18249396
19	3	20.08553692
20	3.5	33.11545196
21	4	54.59815003
22	4.5	90.0171313
23	5	148.4131591
24	5.5	244.6919323
25	6	403.4287935

Entry mode Initial segment

Track the error on the intermediate calculation steps:



$$V_1 := 5$$

$$V_2 := 1.75$$

$$\frac{V_1}{V_2} = 2.857$$

$$\ln(V_1) = 1.609$$

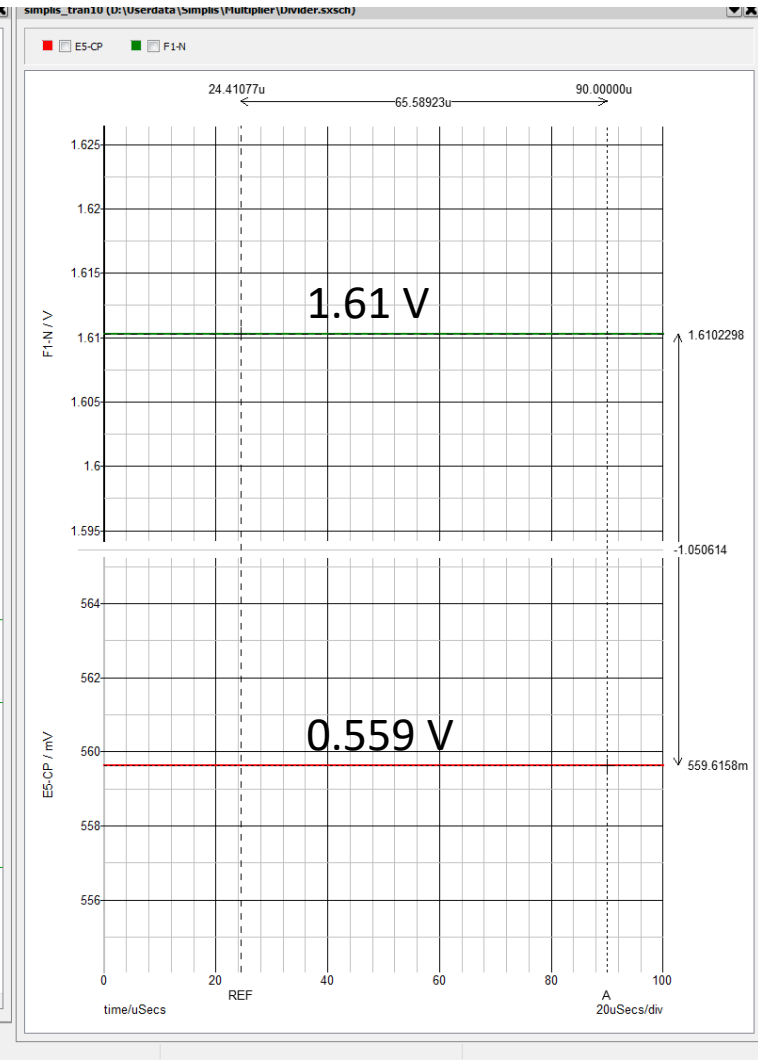
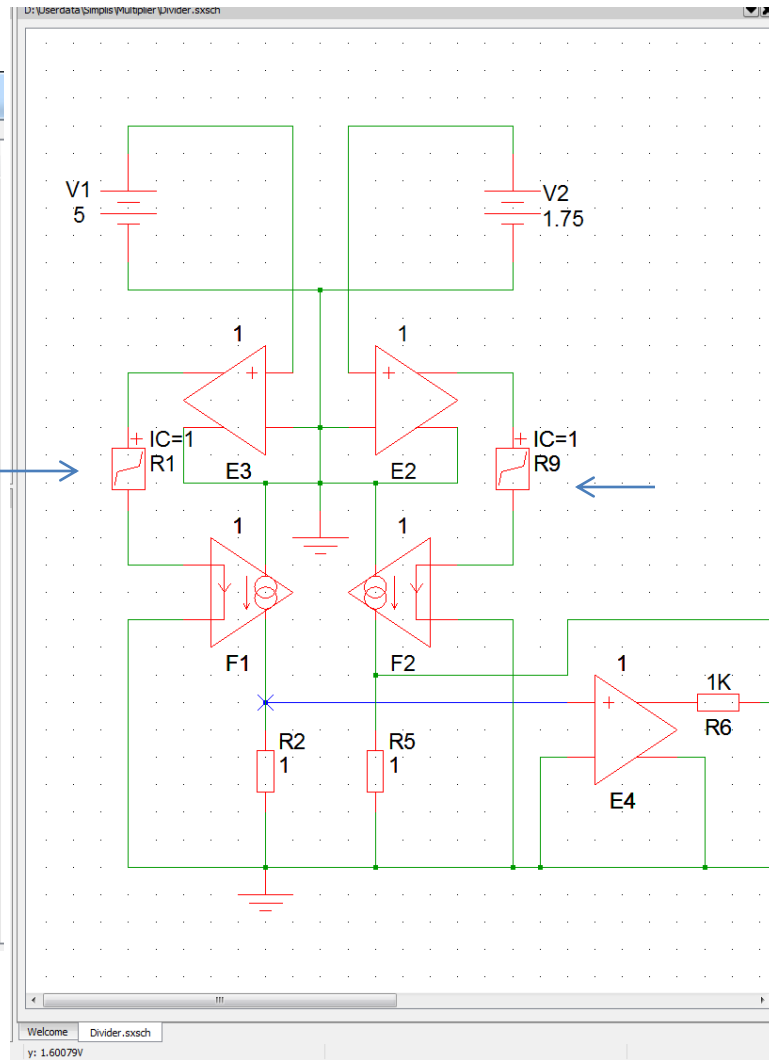
$$\ln(V_2) = 0.56$$

$$\ln(V_1) - \ln(V_2) = 1.05$$

Resolution is increased to 50 data points with 100-mV steps

Define VPWL Resistor: R9

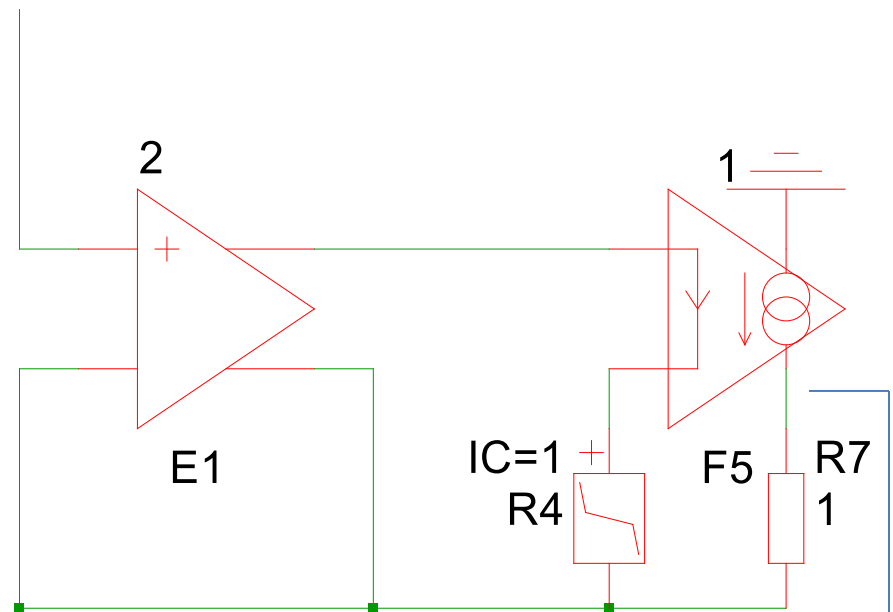
	Voltage	Current
1	5.00E-02	-2.995732274
2	1.50E-01	-1.897119985
3	2.50E-01	-1.386294361
4	3.50E-01	-1.049822124
5	4.50E-01	-0.798507696
6	5.50E-01	-0.597837001
7	6.50E-01	-0.430782916
8	7.50E-01	-0.287682072
9	8.50E-01	-0.162518929
10	9.50E-01	-0.051293294
11	1.05E+00	0.048790164
12	1.15E+00	0.139761942
13	1.25E+00	0.223143551
14	1.35E+00	0.300104592
15	1.45E+00	0.371563556
16	1.55E+00	0.438254931
17	1.65E+00	0.500775288
18	1.75E+00	0.559615788
19	1.85E+00	0.615185639
20	1.95E+00	0.667829373
21	2.05E+00	0.717839793
22	2.15E+00	0.765467842
23	2.25E+00	0.810930216
24	2.35E+00	0.854415328
25	2.45E+00	0.895000000



Increase the granularity for the last resistor to 120 data points

Define VPWL Resistor: R4

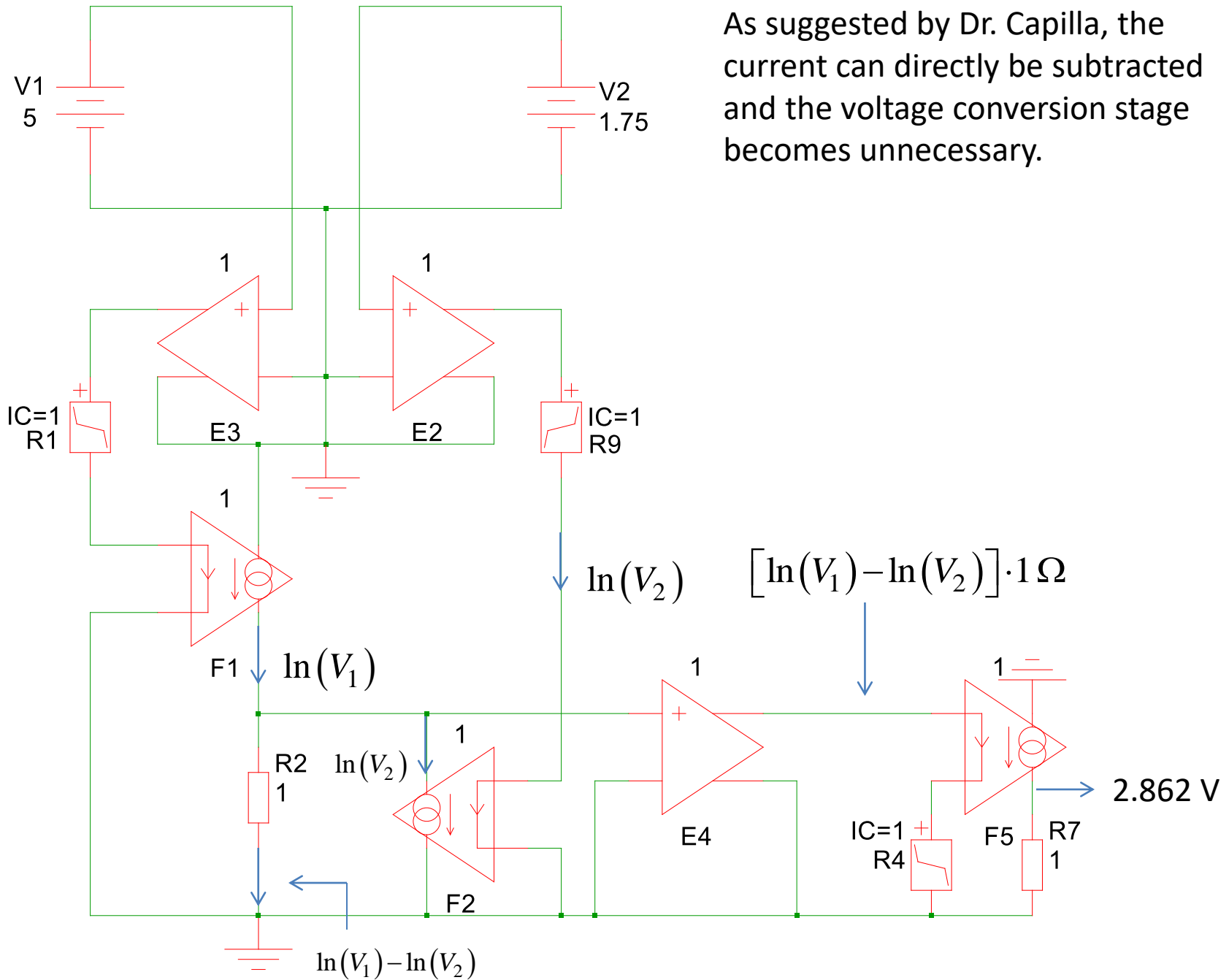
	Voltage	Current
1	-6	0.002478752
2	-5.9	0.002739445
3	-5.8	0.003027555
4	-5.7	0.003345965
5	-5.6	0.003697864
6	-5.5	0.004086771
7	-5.4	0.004516581
8	-5.3	0.004991594
9	-5.2	0.005516564
10	-5.1	0.006096747
11	-5	0.006737947
12	-4.9	0.007446583
13	-4.8	0.008229747
14	-4.7	0.009095277
15	-4.6	0.010051836
16	-4.5	0.011108997
17	-4.4	0.01227734
18	-4.3	0.013568559
19	-4.2	0.014995577
20	-4.1	0.016572675
21	-4	0.018315639
22	-3.9	0.020241911
23	-3.8	0.022370772
24	-3.7	0.024723526
25	-3.6	0.027303333



$$\frac{5}{1.75} = 2.857$$

$$\frac{5}{1.75} \rightarrow 2.862$$

As suggested by Dr. Capilla, the current can directly be subtracted and the voltage conversion stage becomes unnecessary.



Math operations between dynamic signals in Simplis require the usage of log functions that are summed or subtracted. The result is then conveyed through an exponential expression to obtain the final result.

It is important to correctly assess the signal dynamics when configuring the VPWL resistors. Increasing the number of segments is better for precision but detrimental to simulation speed: some tradeoff is necessary here.