GaN-Based 250-kHz LLC Converter with Hybrid Analogue-Digital Control

Christophe Basso[1], Josef Burger[2], David Woodcock[2], Zhi Zhang[2]

[1] Future Electronics, Colomiers, France

[2] Future Electronics, Centre of Excellence, Egham, UK

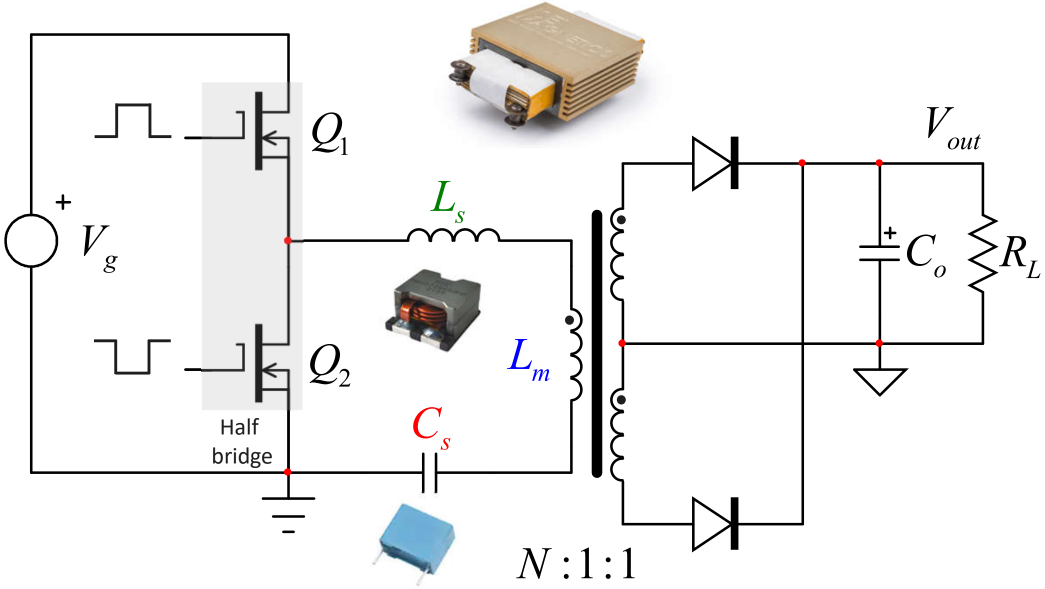
April 2023 – Rev 0.16

Agenda

- The LLC Converter
- Controlling the Power Flow
- A Closed-Loop Control System
- Bringing a Microcontroller on Board
- Combining Analogue and Digital
- Practical Implementation
- Conclusion

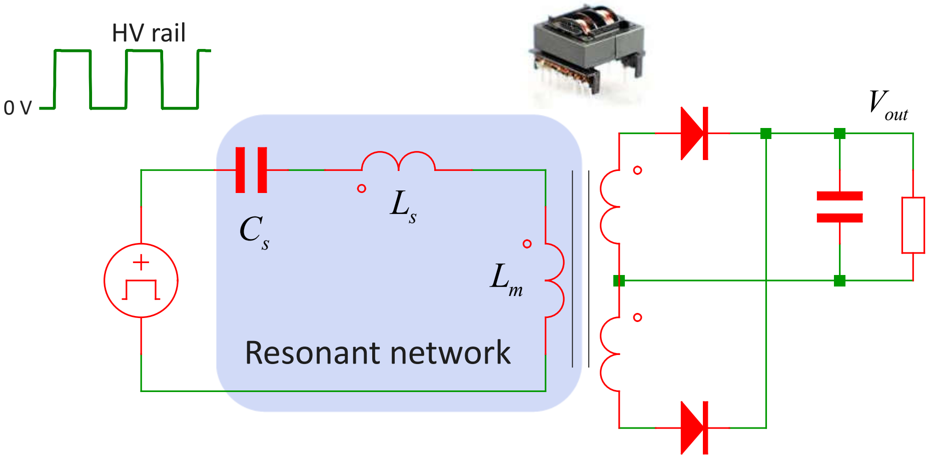
What is an LLC Converter?

- The LLC converter is a member of the series-resonant converters family
  - ➢ The magnetizing inductance L_m is part of the resonating elements (L)
  - ➢ The transformer leakage inductance or an extra inductor forms the term L_s (L)
  - ➢ A series capacitor C_s is inserted to form the complete resonant converter (C)



The Benefits of the LLC Converter

- The LLC converter offers soft-switching conditions in normal-load conditions
  - ✓ Zero-voltage switching (ZVS) for the switches in the primary side
  - ✓ Zero-current switching (ZCS) for the secondary-side diodes
- It can operate at high switching frequency to build compact converters
  - ✓ Perfect for flat-panel displays like LCD TVs, game stations, servers power supplies

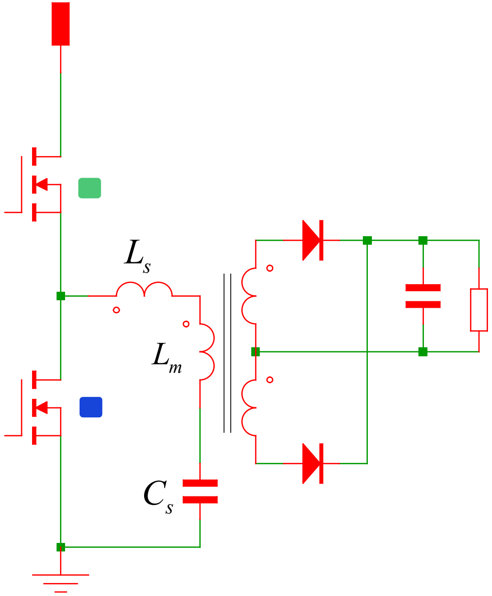


✓ Three energy-storing elements, C_s, L_s and the transformer magnetizing inductance L_m

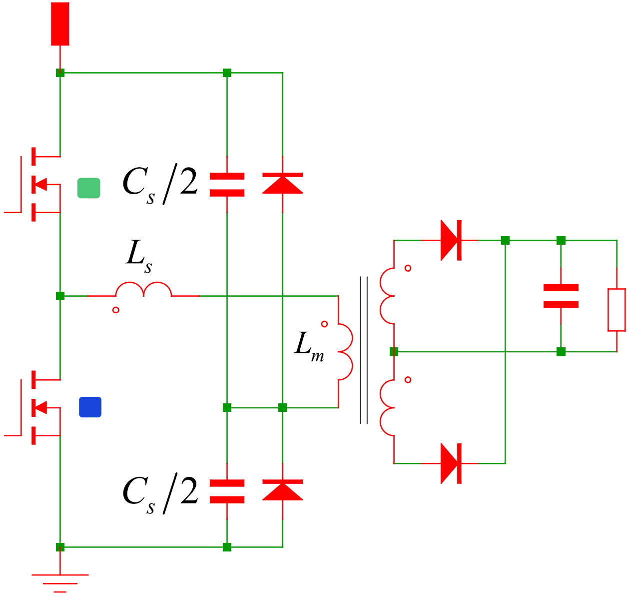
✓ Components count is limited especially if integrated magnetics is adopted

Different Configurations for the LLC - Primary

- The LLC converter can be operated in half- or full-bridge configuration



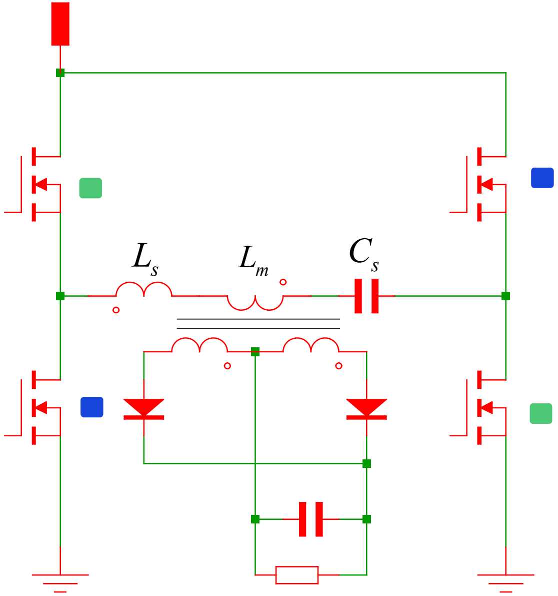
- Power up to 600 W



- Robust version with clamp diodes

✓ Lower input ripple current

✓ Half rms current in a capacitor

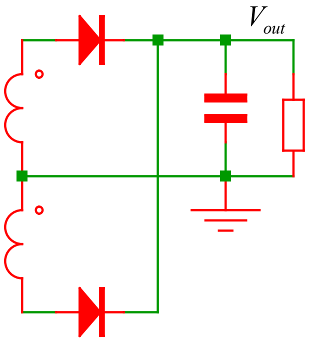


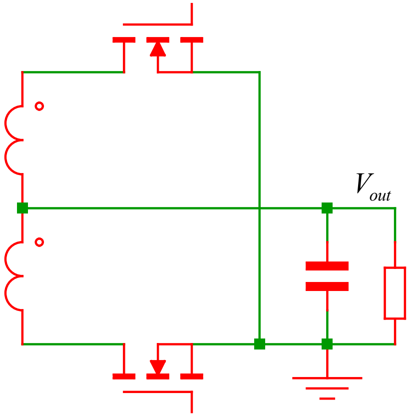
- Power beyond 1 kW

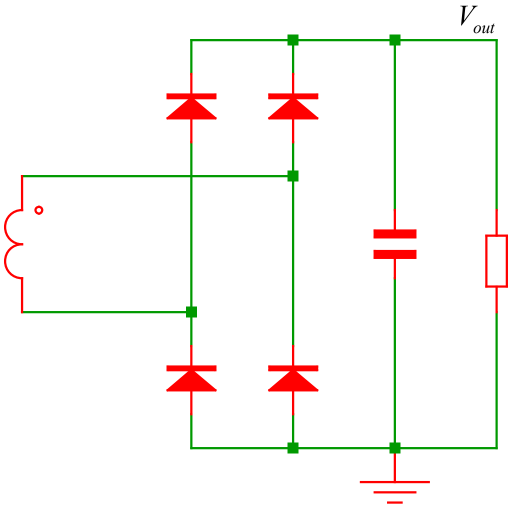
✓ Diagonal conduction

Different Configurations for the LLC - Secondary

- A full-bridge rectifier requires diodes with a lower breakdown voltage







- Two separate windings
- BV > $2V_{out}$
- Secondary leakage brings current imbalance

- Synchronous rectification

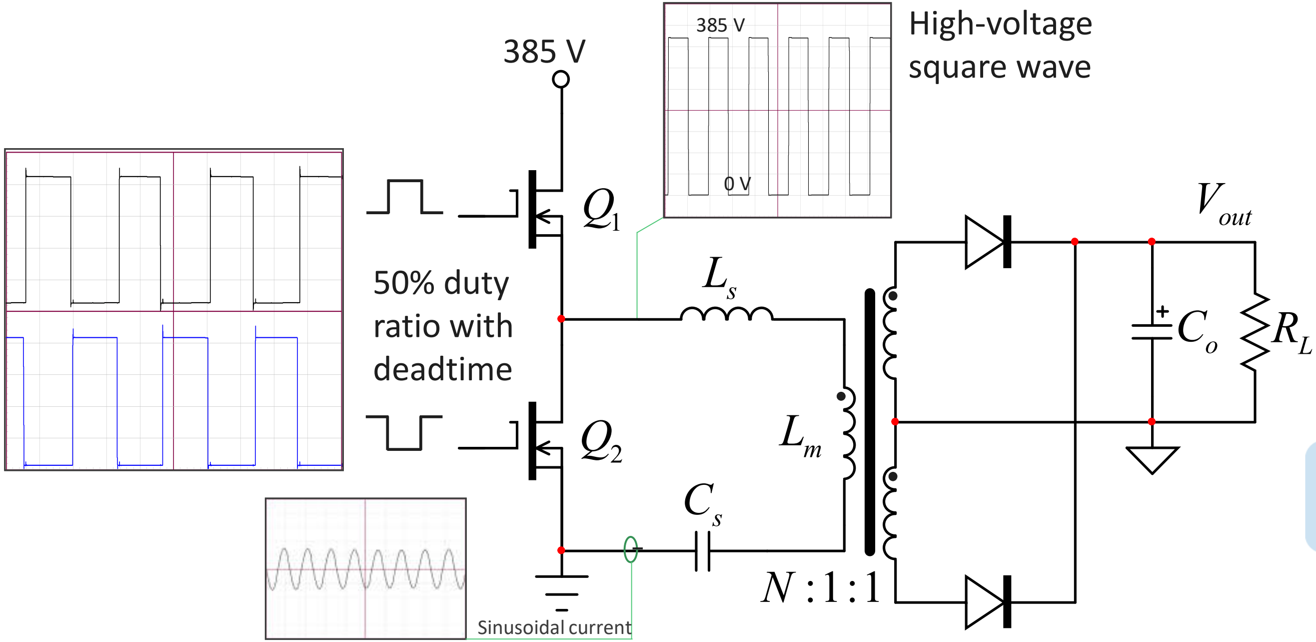
- One single winding
- BV > V_{out}
- No current imbalance

Agenda

- The LLC Converter
- Controlling the Power Flow
- A Closed-Loop Control System
- Bringing a Microcontroller on Board
- Combining Analogue and Digital
- Practical Implementation
- Conclusion

Direct Frequency Control

- An LLC converter is typically operated from a 50% high-voltage square waveform
  - The power flow is then adjusted by varying the switching frequency
  - Soft-switching on MOSFETs and diodes depends on frequency with respect to f_s



High-voltage square wave

50% duty ratio with deadtime

Sinusoidal current

High power

$$f_s = \frac{1}{2\pi\sqrt{L_s C_s}}$$

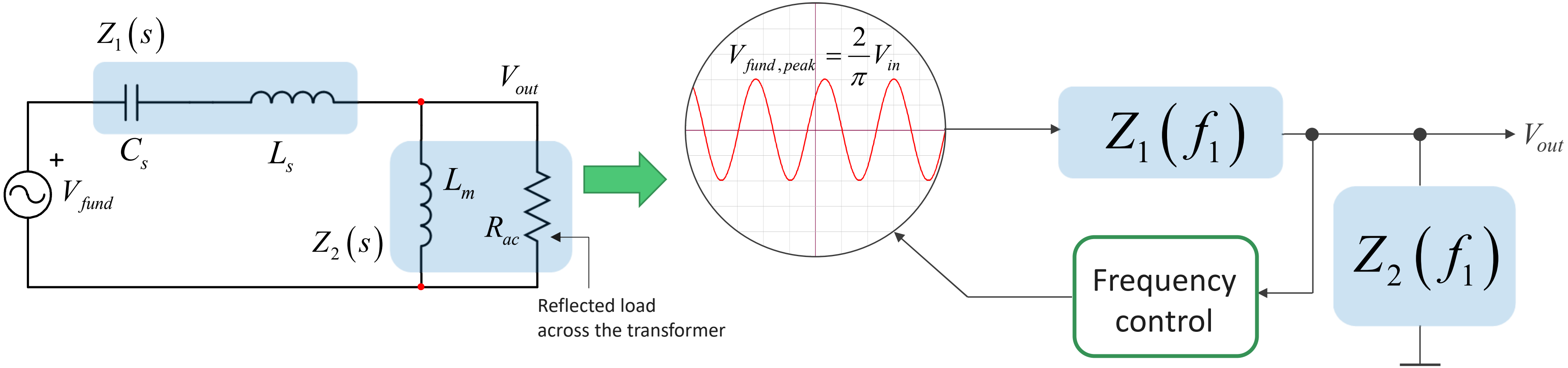
A multi-resonance system

$$f_m = \frac{1}{2\pi\sqrt{(L_s + L_m)C_s}}$$

Low power

The Resonance varies with the Output Power

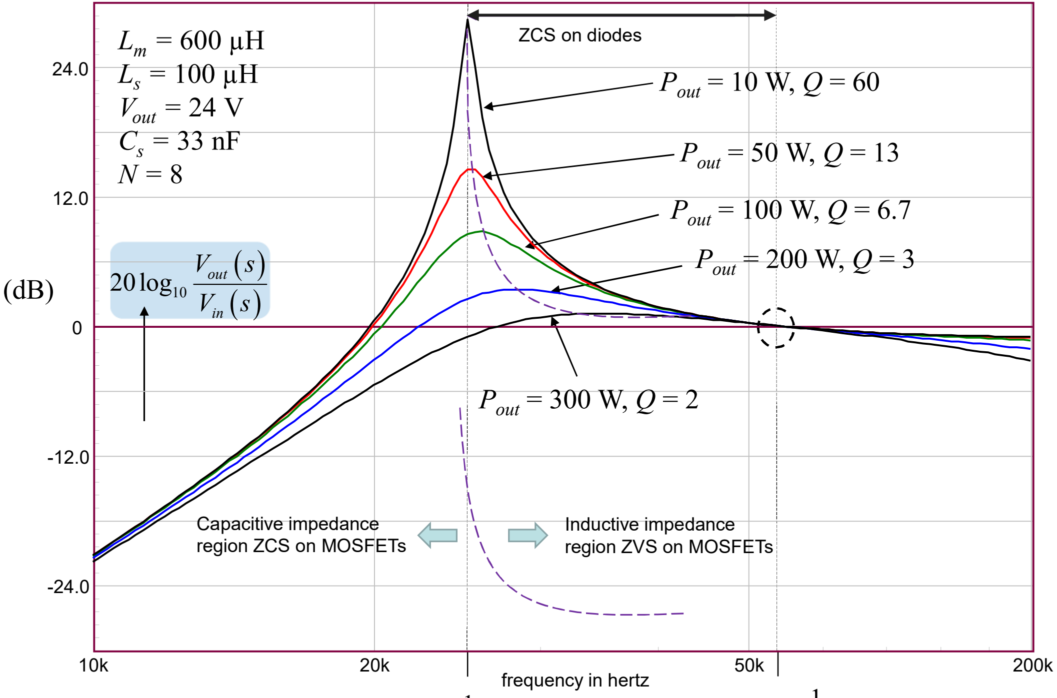
- The LLC converter is a multi-resonance converter depending on operating conditions
  - In heavy-load condition, L_s dominates the resonant tank as L_m is shunted by R_{ac}
  - In lighter-load operations, L_m and L_s together set the resonant frequency



- The converter is modeled using the first harmonic approximation or FHA

Where to Operate the Converter?

- Plotting the dc transfer characteristic of the LLC network reveals several points



$$F_{\min} = \frac{1}{2\pi\sqrt{(L_s + L_m)C_s}}$$

$$F_o = \frac{1}{2\pi\sqrt{L_s C_s}}$$

- ✓ As load current decreases, L_m enters the picture and brings a second peak
- ✓ An impedance plot shows so-called ***capacitive*** and ***inductive*** regions
- ✓ The inductive region brings ZVS on power MOSFETs and ZCS on output diodes
- ✓ ZCS on MOSFETs is occurring in the capacitive region but the control law changes!

Output Voltage of an LLC Converter

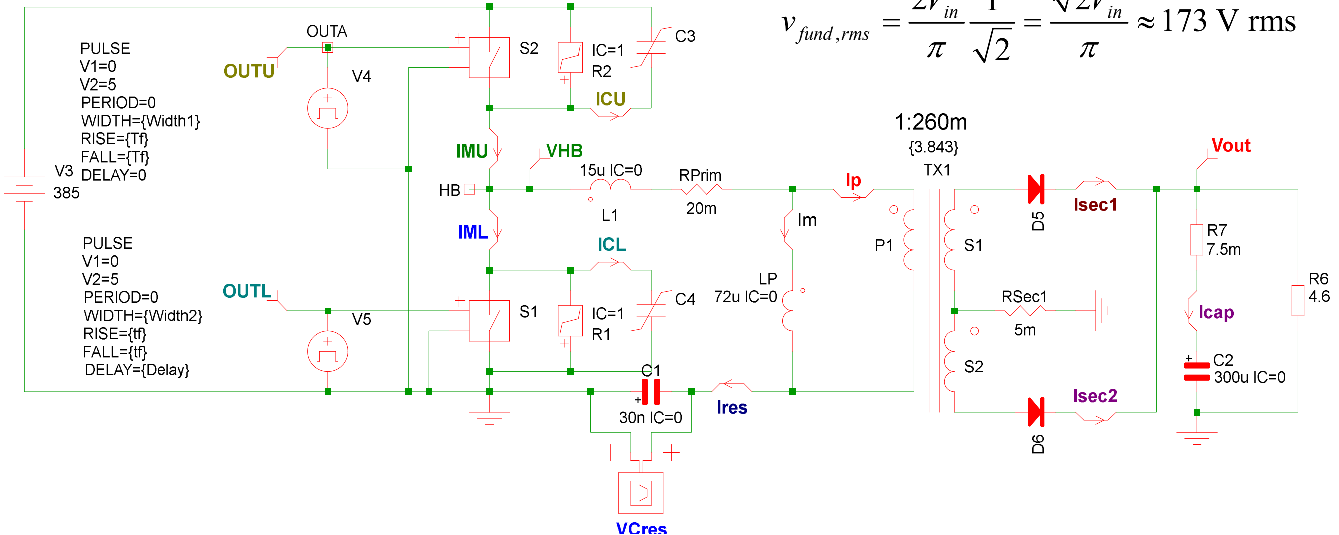
- The equivalent network is fed by the square-wave fundamental value according to FHA
- ✓ Determine the output voltage with the transfer function of the 3rd-order network

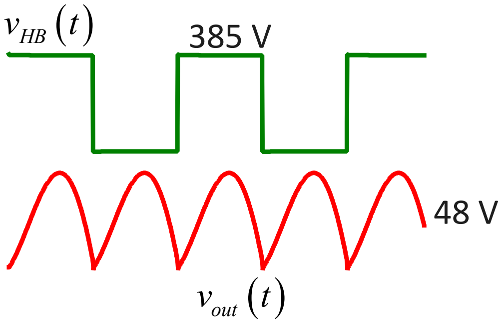
$$H_{m1}(s) := \frac{1}{N_{ps}} \cdot \frac{\frac{L_3}{L_2} \cdot \left(\frac{s}{\omega_s}\right)^2}{1 + s \cdot \frac{L_3}{R_1} + \left(\frac{s}{\omega_m}\right)^2 + s^3 \cdot \frac{L_3}{L_2 \cdot Q_1 \cdot \omega_s^{3}}}$$

$$V_{out} := V_{fund} \cdot \left| H_{ref}(i \cdot 2\pi \cdot F_{sw}) \right| = 45.19774V$$

$$\uparrow$$

$$v_{fund,rms} = \frac{2V_{in}}{\pi} \frac{1}{\sqrt{2}} = \frac{\sqrt{2}V_{in}}{\pi} \approx 173 \text{ V rms}$$



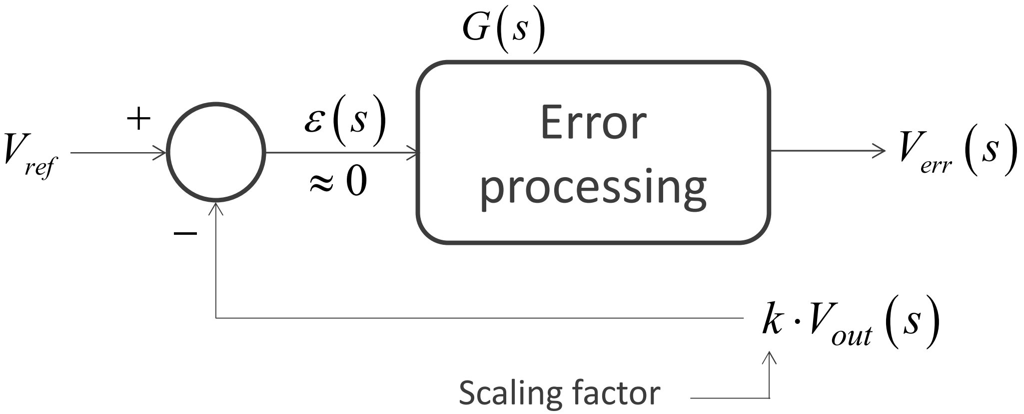


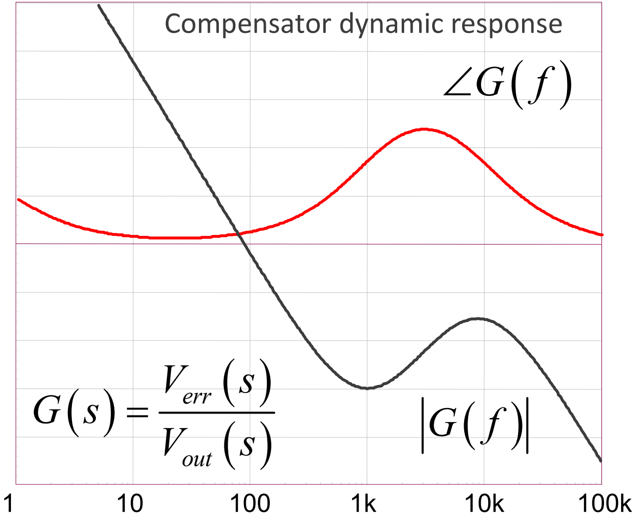
Agenda

- The LLC Converter
- Controlling the Power Flow
- A Closed-Loop Control System
- Bringing a Microcontroller on Board
- Combining Analogue and Digital
- Practical Implementation
- Conclusion

Shaping the Loop with the Compensator

- The compensator builds the error variable and ensures stability
  - ➢ Insert poles and zeros to create the compensation strategy
  - ➢ Choose how to cross over at f_c with phase and gain margins

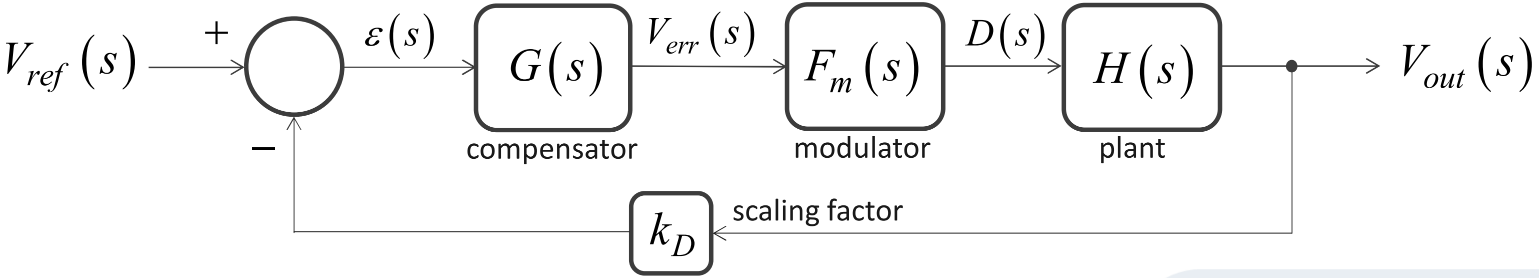




- The block amplifies and shapes the error ε between V_{ref} and V_{out}
  - ✓ Minimize the error between the setpoint and the output

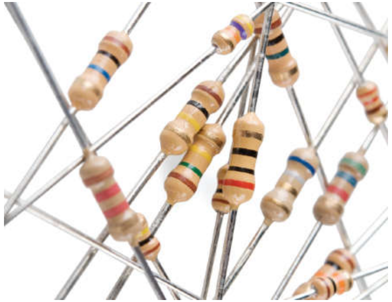
Building the Compensator – the Analogue Way

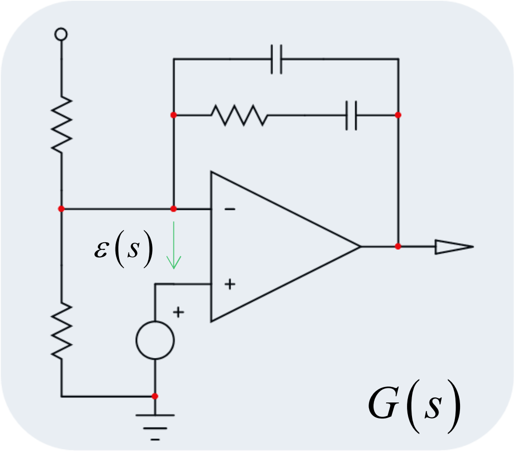
- Associate active and passive components to form the compensation chain



1. Select poles/zeroes placement
2. Calculate components values
3. Solder resistors and capacitors

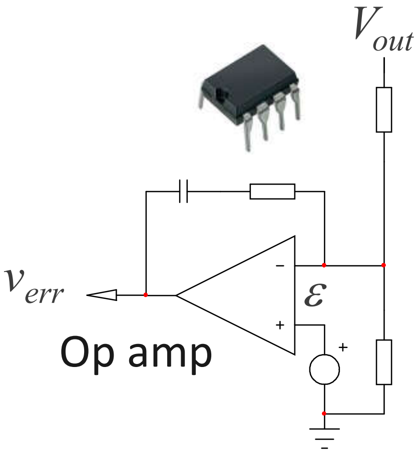
Change in strategy requires new components values

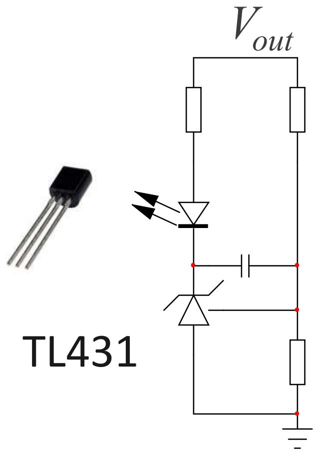


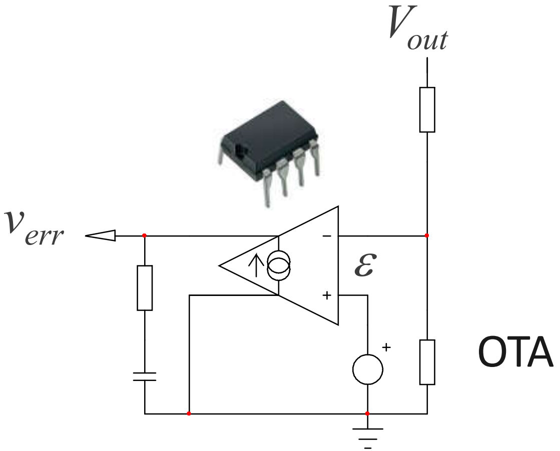


How do you Build an Analogue Compensator?

- A compensator can be a passive or active filter shaped for a specific response

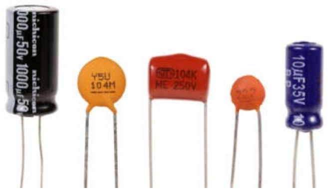






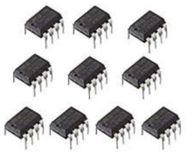
✓ Passive components suffer drawbacks:

1. Tolerance, aging
2. Sensitivity to temperature, humidity



✓ Active components are not perfect!

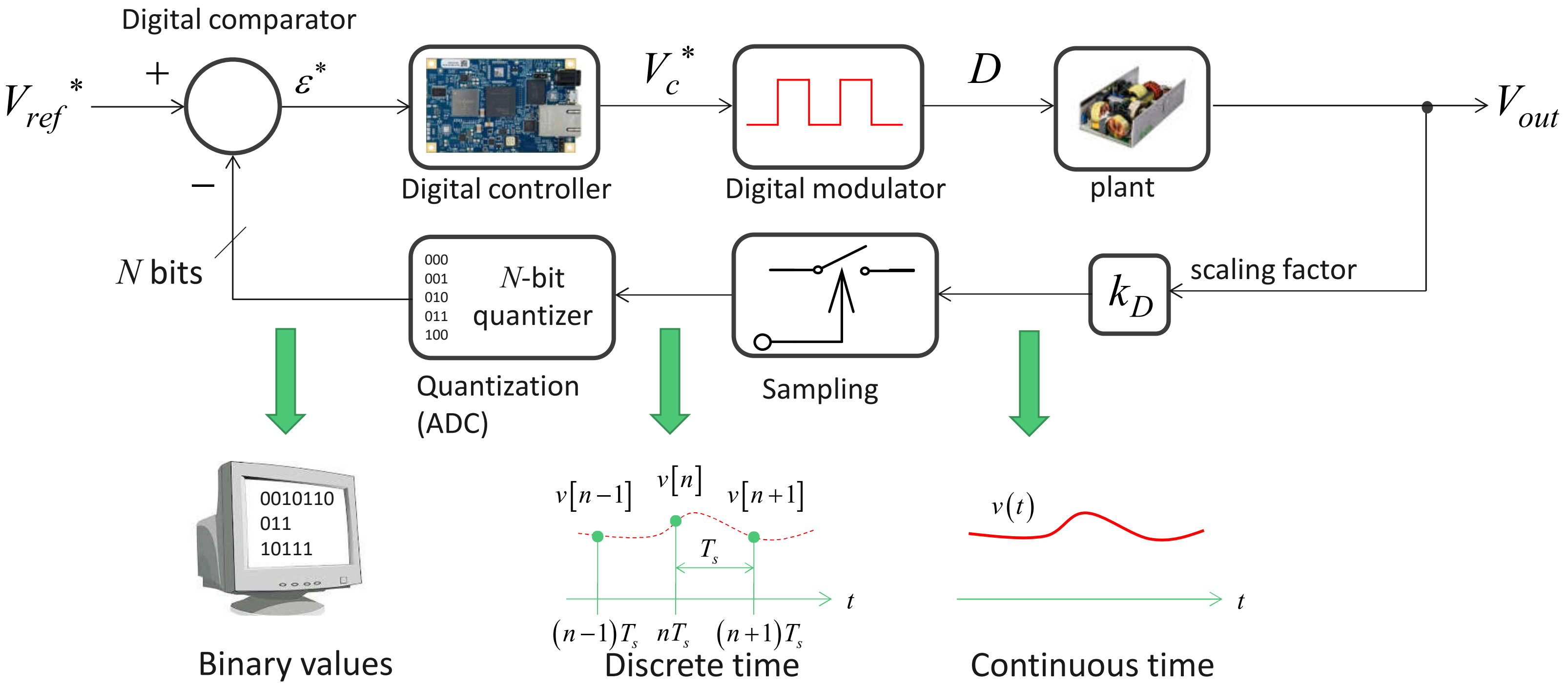
1. Open-loop gain, bias requirements
2. Limited in bandwidth, slew-rate
3. Temperature drift



OTA: operational transconductance amplifier

Building the Compensator – the Digital Way

- A digitally-controlled system mixes sampled and continuous-time data



Digital comparator

V_{ref}^* $+$ $-$ ε^*

Digital controller

V_c^*

Digital modulator

D

plant

V_{out}

scaling factor

k_D

Sampling

N-bit quantizer

000 001 010 011 100

Quantization (ADC)

N bits

0010110 011 10111

Binary values

$v[n-1]$ $v[n]$ $v[n+1]$ T_s t

$(n-1)T_s$ nT_s $(n+1)T_s$

Discrete time

$v(t)$ t

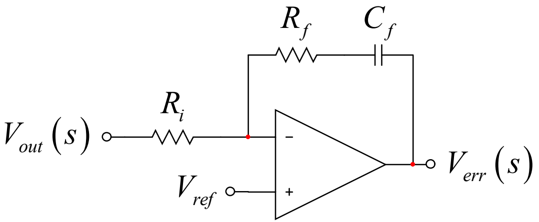
Continuous time

* designates a discrete variable

M. Jovanović, *Introduction to Digital Control of Switch-Mode Converters*, in-house course, PHX 2014

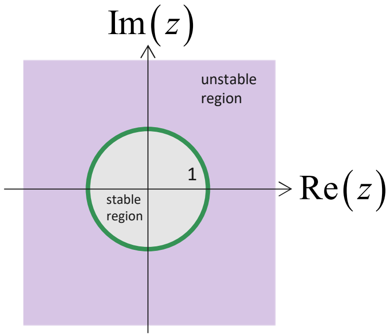
How do you Implement a Digital Compensator?

- You can start from a continuous-time transfer function expressed in s



$$sV_{err}(s) = -s\frac{R_f}{R_i}V_{out}(s) - \frac{1}{R_iC_f}V_{out}(s)$$

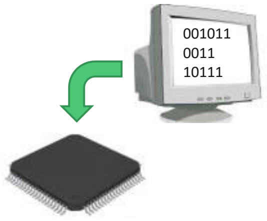
Map into the z-domain



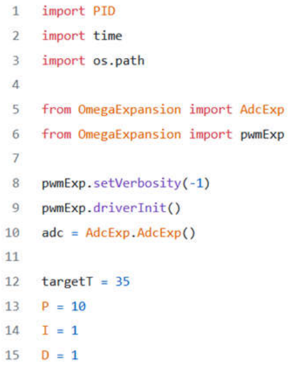
Difference equation

$$b_0V_{err}(z) + b_1z^{-1}V_{err}(z) = a_0V_{out}(z) + a_1z^{-1}V_{err}(z)$$

- Code the filter equation with a micro-controller or hard-wire it in a FPGA



Digital control



```
import PID
import time
import os.path

from OmegaExpansion import AdcExp
from OmegaExpansion import pwmExp

pwmExp.setVerbosity(-1)
pwmExp.driverInit()
adc = AdcExp.AdcExp()

targetT = 35
P = 10
I = 1
D = 1
```

✓ No tolerance or age issues
✓ Flexibility and optimization
✓ On-the-fly poles-zeroes changes
❖ More complex to analyze
❖ Warping occurs during mapping
❖ Lower crossover systems

Learning curve

Agenda

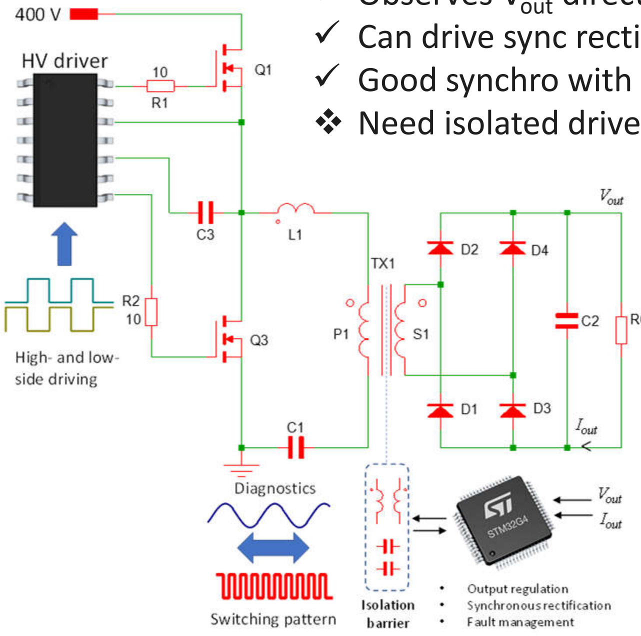
- The LLC Converter
- Controlling the Power Flow
- A Closed-Loop Control System
- Bringing a Microcontroller on Board
- Combining Analogue and Digital
- Practical Implementation
- Conclusion

Where to install the Microcontroller?

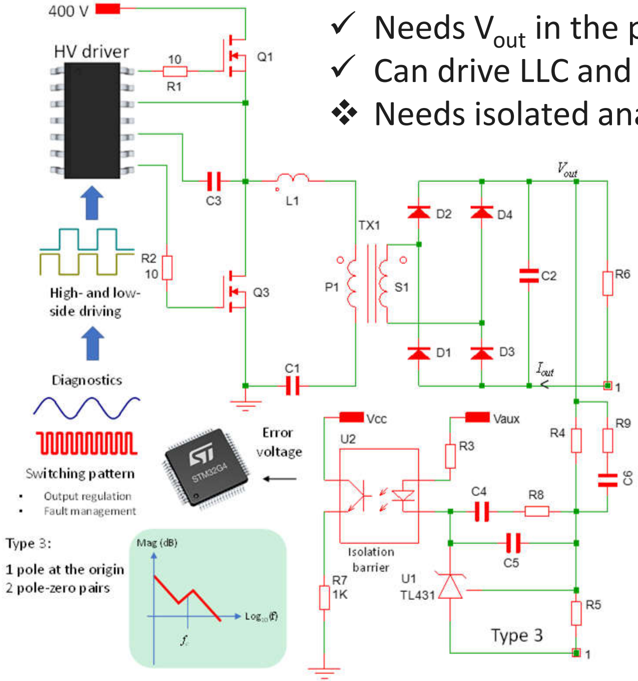
- The component can be placed in the secondary- or primary-side of the converter

✓ *Secondary side* gives access to V_{out} and sync rect control – how to drive HV MOSFETs?

✓ *Primary side* drives and monitors MOSFETs directly but needs isolated access to V_{out}



✓ Observes V_{out} directly
✓ Can drive sync rectifier
✓ Good synchro with prim. side
❖ Need isolated drivers



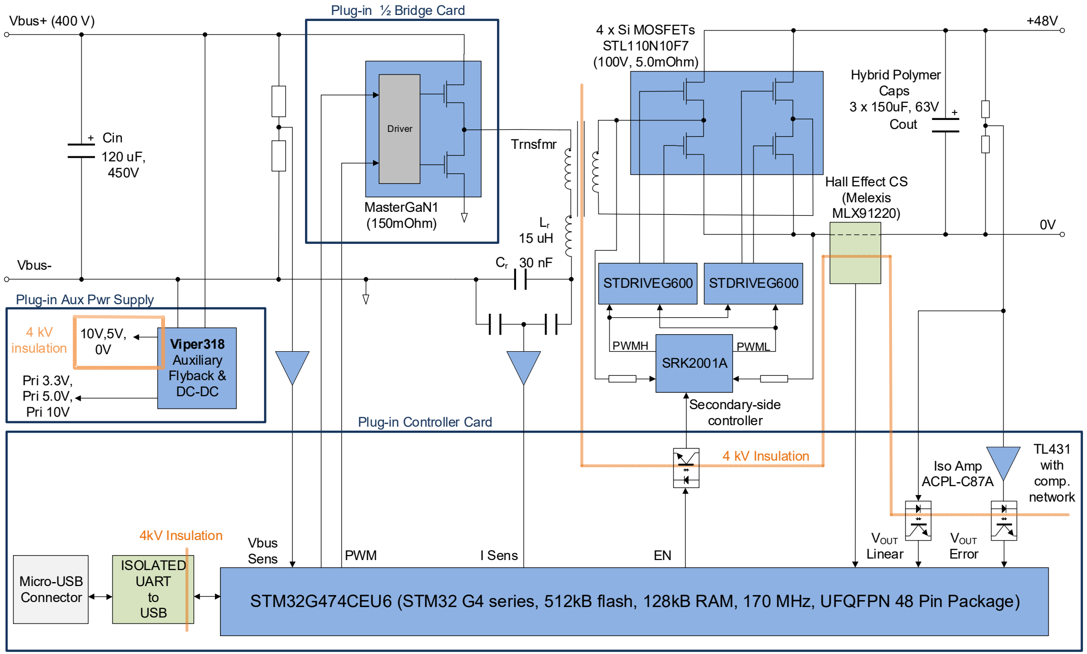
✓ Needs V_{out} in the primary side
✓ Can drive LLC and PFC
❖ Needs isolated analogue control

A GaN-based 500-W LLC Converter

- The circuit will switch at 250 kHz and deliver 48 V/10 A from a 400-V dc source
- MasterGaN1 integrated half-bridge is used in the primary side
- A STM32G4 will control the operations and ensure regulation

MasterGaN1

STM32G4
512 kB flash
128 kB RAM



Secondary full-bridge synchronous rectification

Optocoupler-based hybrid configuration for the feedback

Isolating the Regulation Path

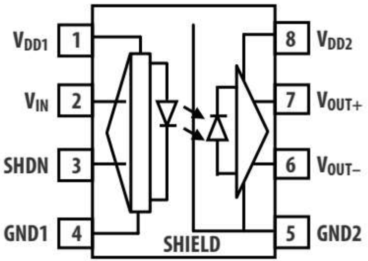
- One easy solution consists of using a fully-isolated linear amplifier

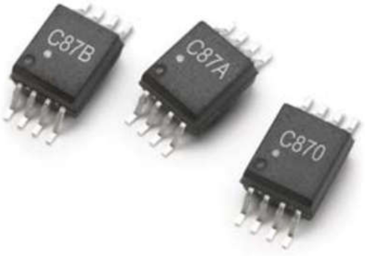
✓ The part exhibits a 100-kHz bandwidth with 1 kV+ isolation voltage

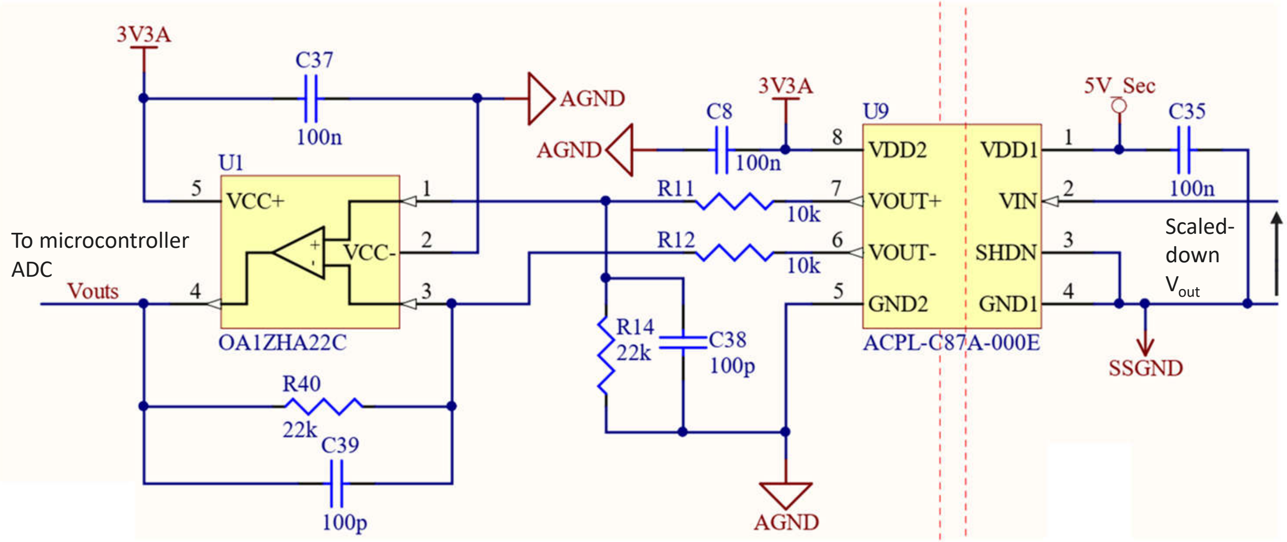
✓ Compact 8-pin package

❖ Cost is high

ACPL-C87A-500E





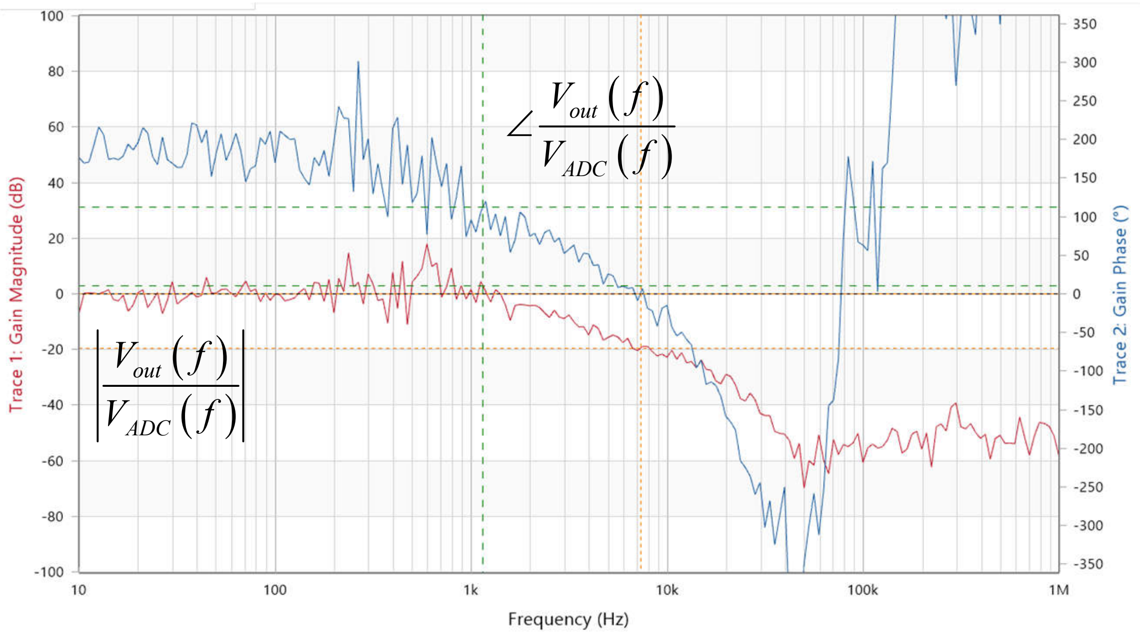


To microcontroller ADC

Scaled-down V_{out}

The Control-to-Output Transfer Function

- This is the starting point for the loop stabilization exercise
- A stimulus is applied to the microcontroller ADC input with $k_d = k_i = 0$
- Coefficient k_p is kept for transmitting the modulation pattern from the FRA



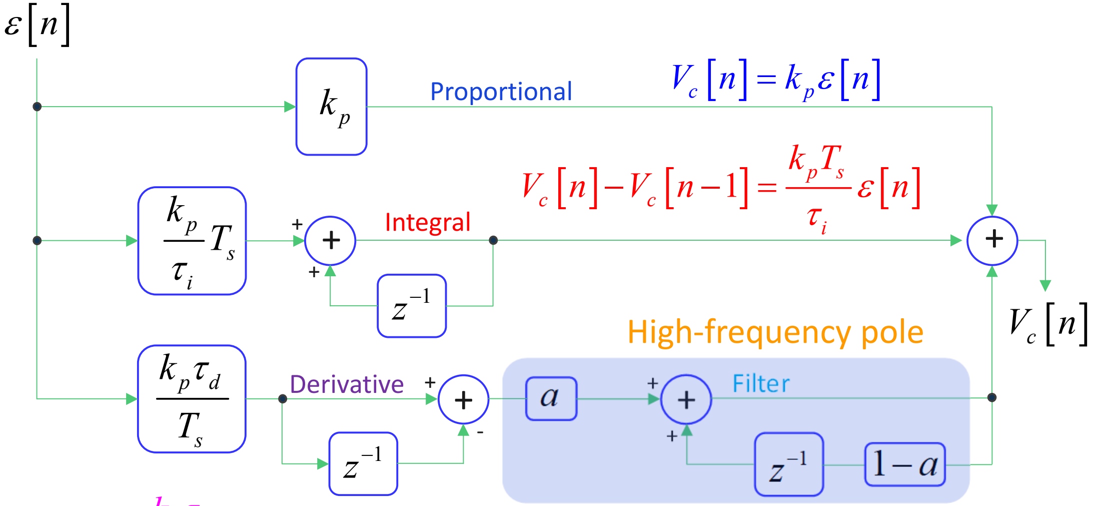
- A *stimulus* is applied at the ADC input
- This stimulus modulates the switching frequency to form a *response*

$$H(s)=\frac{V_{out}(s)}{V_{ADC}(s)}\begin{array}{l}\leftarrow \text{response}\\ \leftarrow \text{stimulus}\end{array}$$

FRA: frequency response analyzer

Discrete Loop Compensation

- The microcontroller implements an unfiltered-PID routine used for the first experiments
- The sampling frequency is 50 kHz and the goal is to crossover at 1 kHz
- A PID is made of several blocks introducing a pole at the origin and two zeroes
  - ➢ These parameters are set by coefficients k_i, k_d and k_p



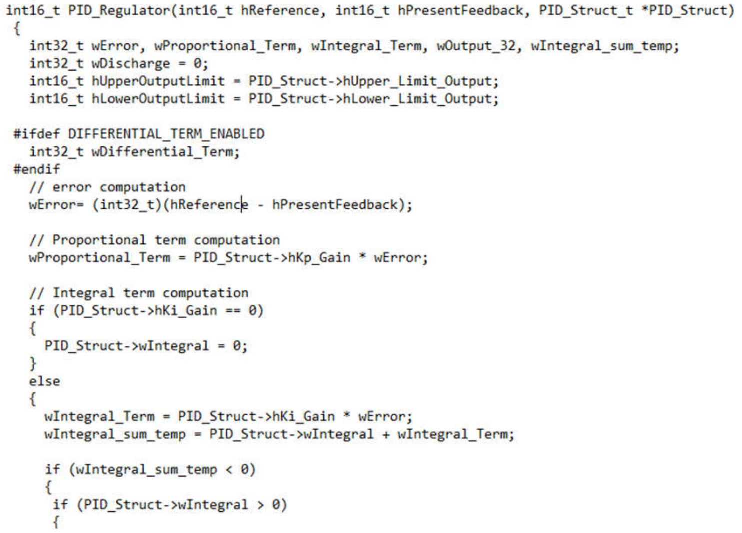
$$V_c[n] = k_p \varepsilon[n]$$

$$V_c[n] - V_c[n-1] = \frac{k_p T_s}{\tau_i} \varepsilon[n]$$

$$V_c[n] = \frac{k_p \tau_d}{T_s}\left(\varepsilon[n] - \varepsilon[n-1]\right)$$

$$V_c[n] = a \cdot \varepsilon_2[n] + V_c[n-1](1-a)$$

Example of code, *PID_regulators.c*, STMicroelectronics

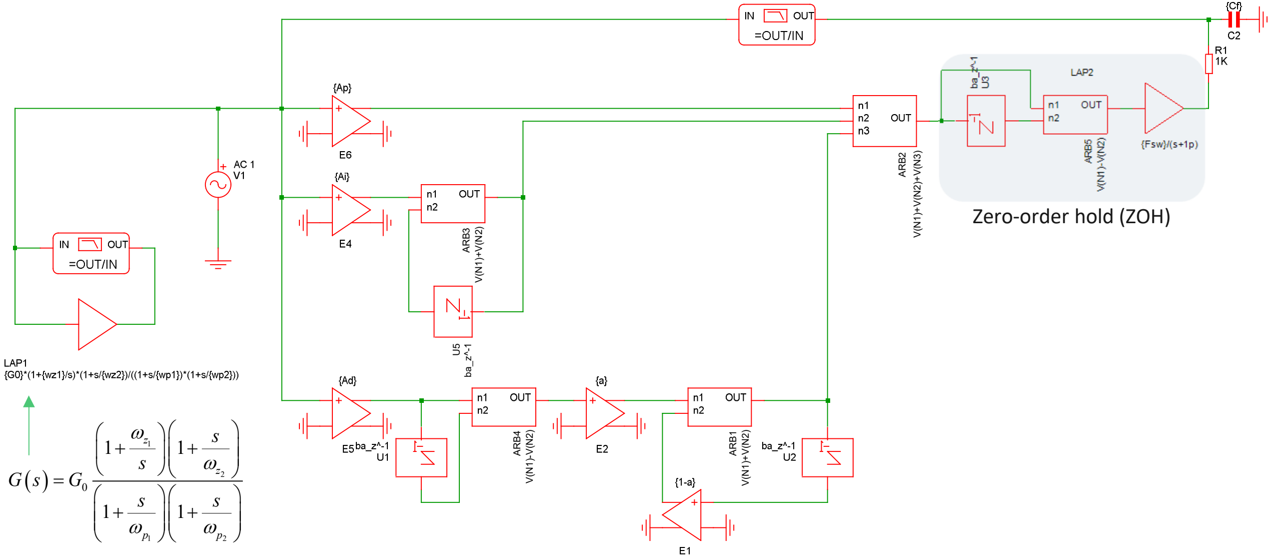


```
int16_t PID_Regulator(int16_t hReference, int16_t hPresentFeedback, PID_Struct_t *PID_Struct)
 {
   int32_t wError, wProportional_Term, wIntegral_Term, wOutput_32, wIntegral_sum_temp;
   int32_t wDischarge = 0;
   int16_t hUpperOutputLimit = PID_Struct->hUpper_Limit_Output;
   int16_t hLowerOutputLimit = PID_Struct->hLower_Limit_Output;

 #ifdef DIFFERENTIAL_TERM_ENABLED
   int32_t wDifferential_Term;
 #endif
   // error computation
   wError= (int32_t)(hReference - hPresentFeedback);

   // Proportional term computation
   wProportional_Term = PID_Struct->hKp_Gain * wError;

   // Integral term computation
   if (PID_Struct->hKi_Gain == 0)
   {
     PID_Struct->wIntegral = 0;
   }
   else
   {
     wIntegral_Term = PID_Struct->hKi_Gain * wError;
     wIntegral_sum_temp = PID_Struct->wIntegral + wIntegral_Term;

     if (wIntegral_sum_temp < 0)
     {
      if (PID_Struct->wIntegral > 0)
      {
```

Convert Poles and Zeroes to Coefficients

- It is advantageous to converter the wanted poles and zeroes to PID coefficients
- Methods like Ziegler-Nichols are based on empirical approach

$$\tau_i = \frac{\omega_{z_1} + \omega_{z_2}}{\omega_{z_1}\omega_{z_2}} - \frac{1}{\omega_{p_1}} \qquad N = \frac{\omega_{p_1}{}^2}{\omega_{p_1}\omega_{z_1} + \omega_{p_1}\omega_{z_2} - \omega_{z_1}\omega_{z_2}} - 1 \qquad k_p = \frac{\omega_{po}}{\omega_{z_1}} - \frac{\omega_{po}}{\omega_{p_1}} + \frac{\omega_{po}}{\omega_{z_2}} \qquad \tau_d = \frac{\left(\omega_{p_1} - \omega_{z_1}\right)\left(\omega_{p_1} - \omega_{z_2}\right)}{\left(\omega_{p_1}\omega_{z_1} + \omega_{p_1}\omega_{z_2} - \omega_{z_1}\omega_{z_2}\right)\omega_{p_1}}$$



$$G(s) = G_0 \frac{\left(1 + \frac{\omega_{z_1}}{s}\right)\left(1 + \frac{s}{\omega_{z_2}}\right)}{\left(1 + \frac{s}{\omega_{p_1}}\right)\left(1 + \frac{s}{\omega_{p_2}}\right)}$$

Reference TF type 3

- Choose poles/zeroes position
- Compute PID coefficients

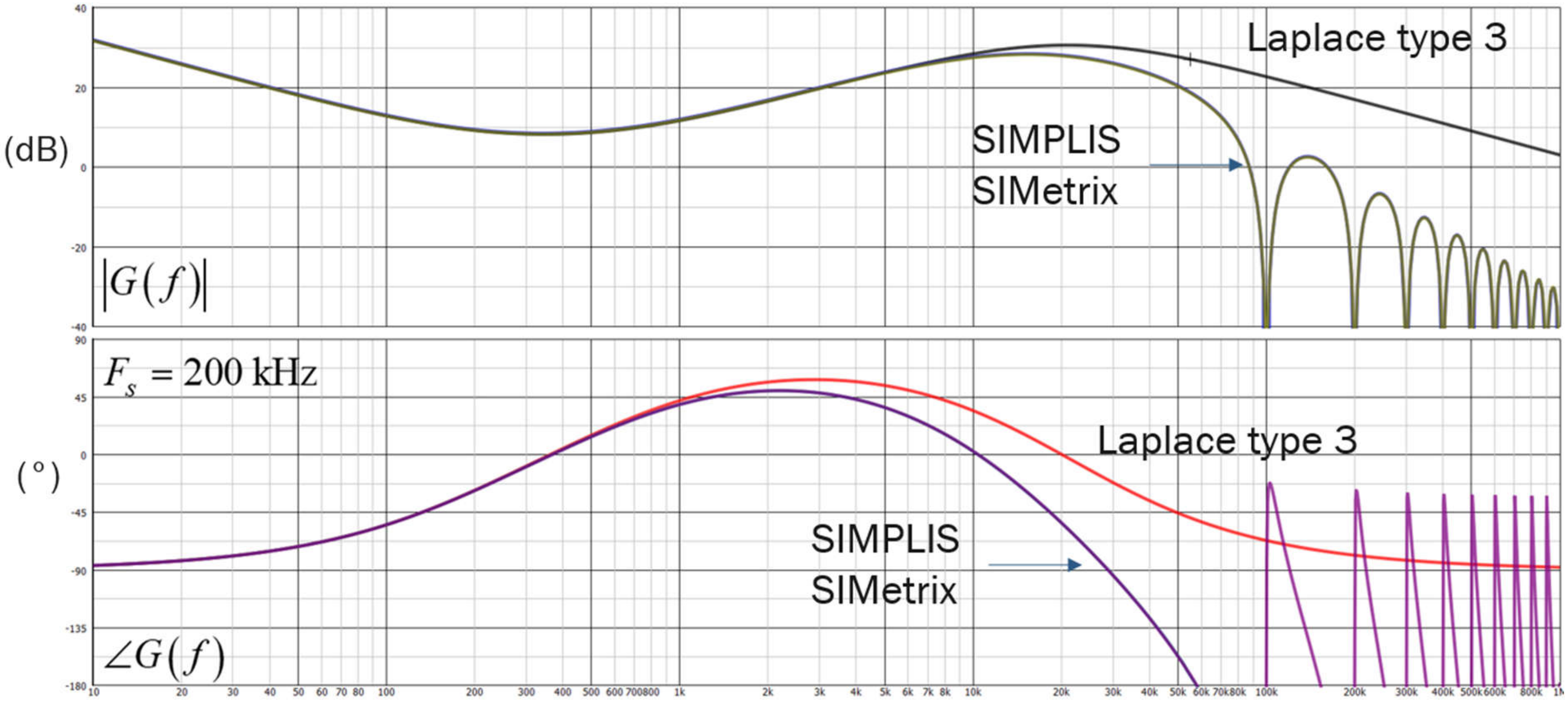
$f_c = 3$ kHz
$G_{f_c} = 20$ dB
$f_{z_1} = 200$ Hz
$f_{z_2} = 600$ Hz
$f_{p_1} = 21$ kHz
$f_{p_2} = 21$ kHz

$\tau_d = 193\ \mu\text{s}$
$N = 26.43$
$\tau_i = 1.053$ ms
$k_p = 2.64$
$A_i = 2.51m$
$A_p = k_p$
$A_d = 509.6$

C. Basso, *Designing Control Loops for Linear and Switching Power Supplies*, Artech House, 2012

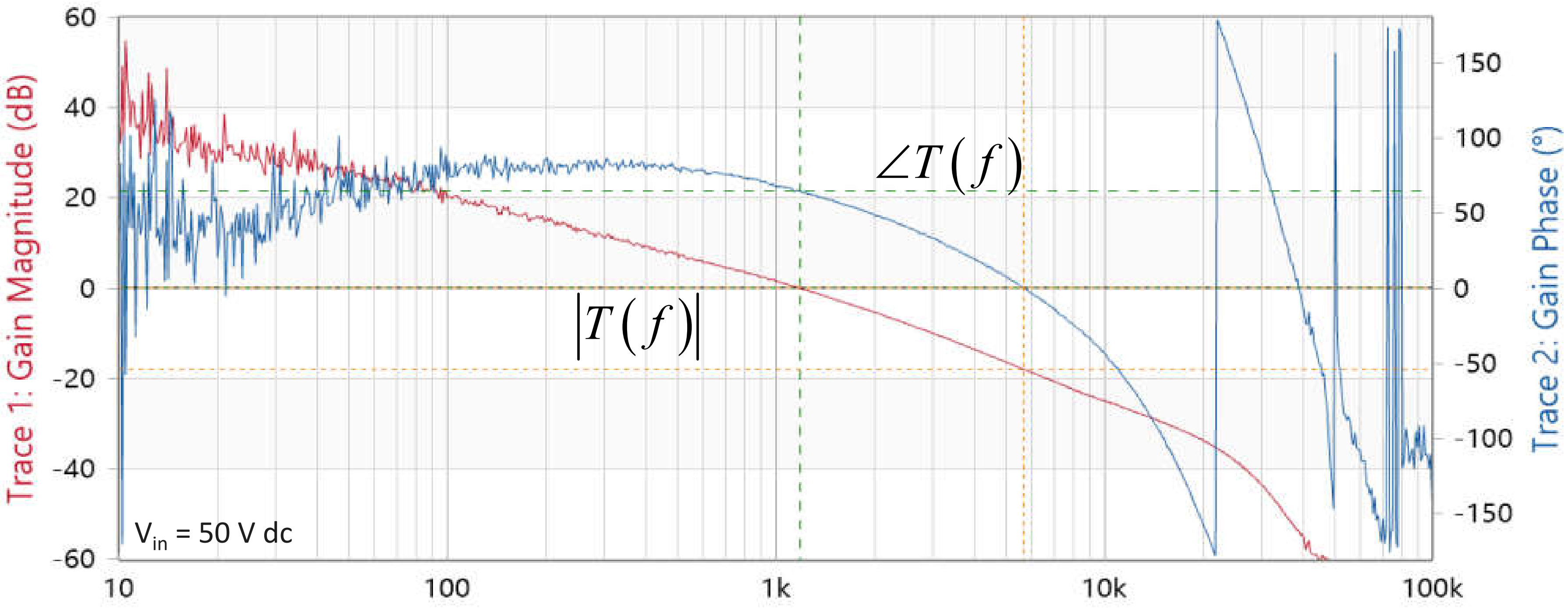
Magnitude and Phase Response of the Discrete PID

- The PID with a second pole shows a response of a type 3 compensator
- The response deviates from the original time-continuous response past a few kHz



Compensated Loop Gain

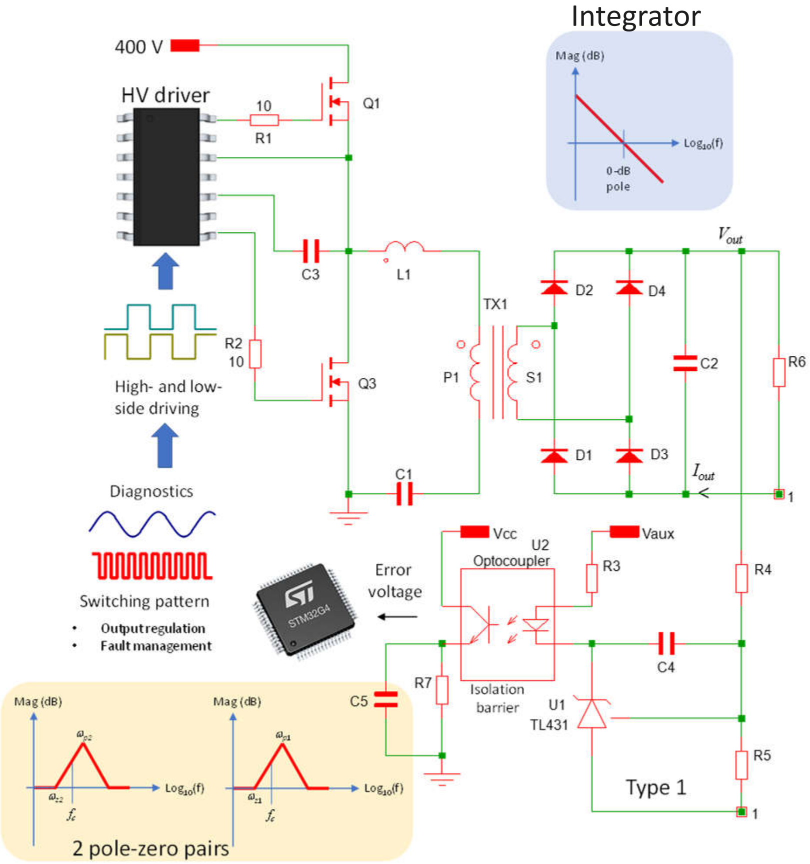
- Computed coefficients lead to a good frequency response for the low-voltage version
- The crossover frequency is slightly above 1 kHz with more than 50° of phase margin



Agenda

- The LLC Converter
- Controlling the Power Flow
- A Closed-Loop Control System
- Bringing a Microcontroller on Board
- Combining Analogue and Digital
- Practical Implementation
- Conclusion

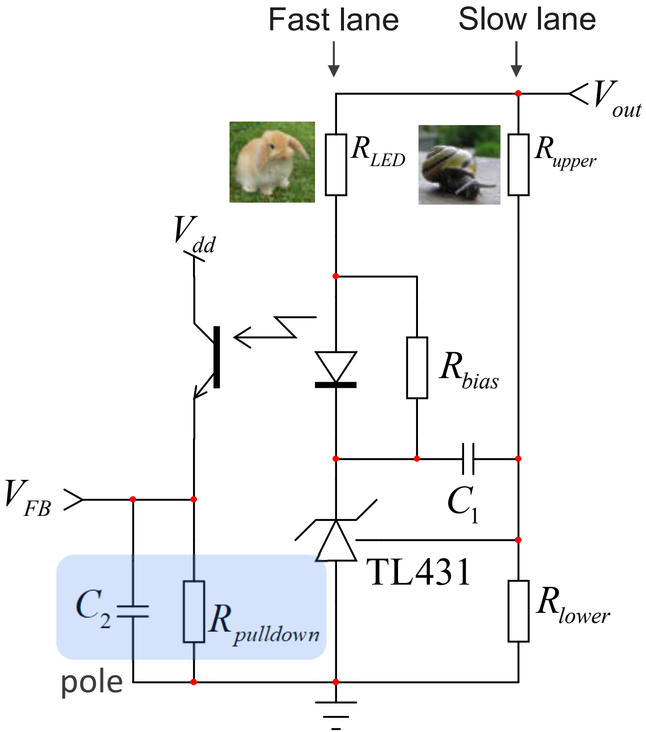
Analogue and Digital Control



- The adopted solution combines an analogue front-end with a digital compensator
- ✓ The analogue section offers a high dc gain with a pole at the origin
- ✓ A low-cost TL431 coupled with an optocoupler transmits the control signal to the ADC
- ✓ The microcontroller implements a two-zero two-pole digital filter
- ✓ Adjusting the distance between the poles and zeroes sizes the phase boost amount

An Isolated Integrator with TL431

- The TL431 configured with a fast lane introduces a zero in the transfer function
- By neutralizing this zero with a pole, an integrator is implemented



$$\frac{V_{FB}(s)}{V_{out}(s)} = -\frac{R_{pulldown}\mathrm{CTR}}{R_{LED}}\left[\frac{\boxed{1+sR_{upper}C_1}}{sR_{upper}C_1\boxed{\left(1+sR_{pulldown}C_2\right)}}\right]$$

$$sR_{upper}C_1 = sR_{pulldown}C_2 \Rightarrow C_1 = \frac{R_{pulldown}}{R_{upper}}C_2$$

$$\omega_{po} = \frac{\mathrm{CTR}}{C_2 R_{LED}} \Rightarrow C_2 = \frac{\mathrm{CTR}}{2\pi f_{po} R_{LED}}$$

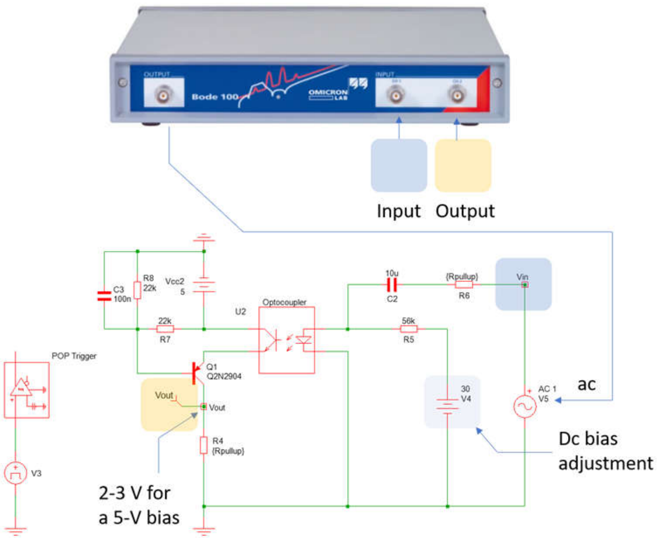
substitute

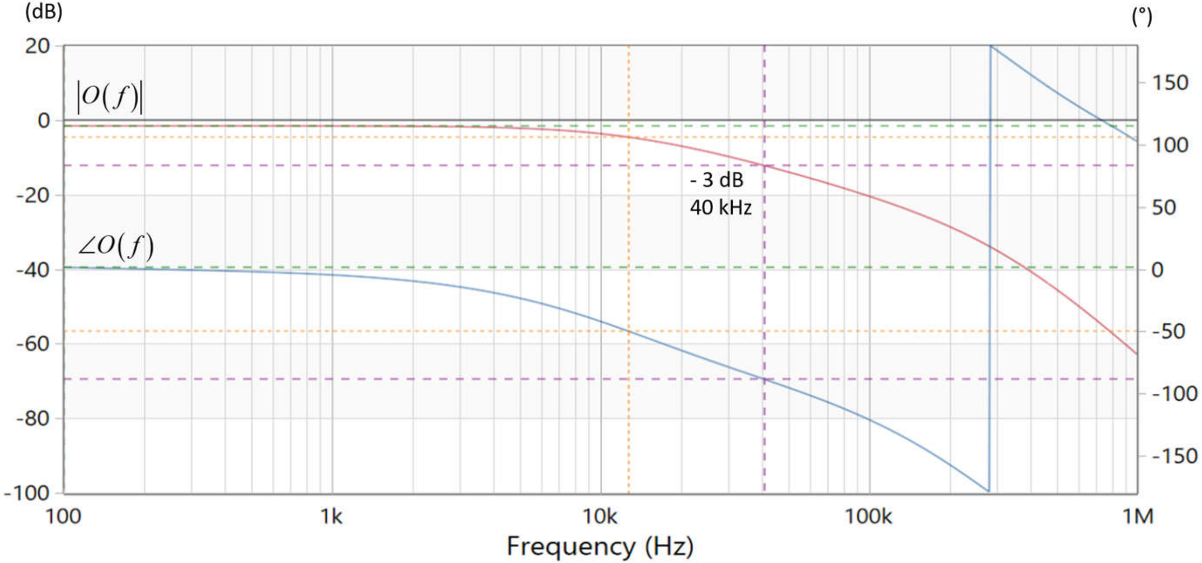
$$\Rightarrow \omega_{po} = \frac{1}{\dfrac{R_{upper}R_{LED}}{R_{pulldown}\mathrm{CTR}}C_1}$$

C. Basso, The TL431 in the Control of Switching Power Supplies, onsemi Asian Seminars 2009

Extending the Optocoupler Bandwidth

- The optocoupler includes a low-frequency pole which hampers the compensation path
- The cascode configuration relegates this pole to higher frequencies



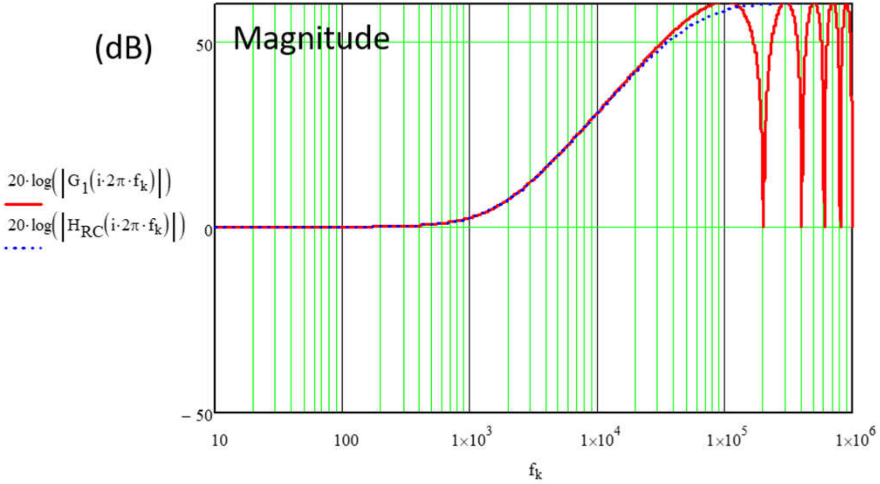


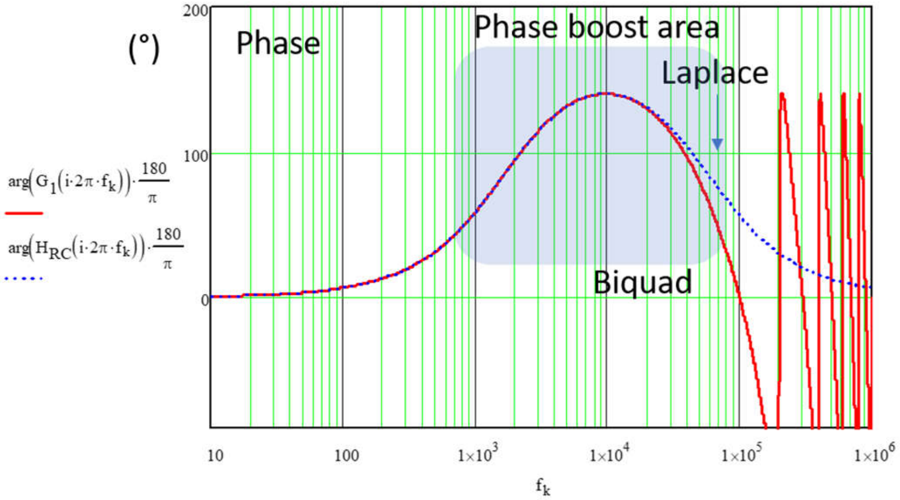
- The pole is located at 40 kHz and would be at ≈4 kHz in classic common-collector circuit

The Digital Filter –Two Pole-Zero Pairs

- A type 3 compensator is realized by cascading the integrator with two pole-zero pairs
- These elements are digitally coded and can later be easily modified

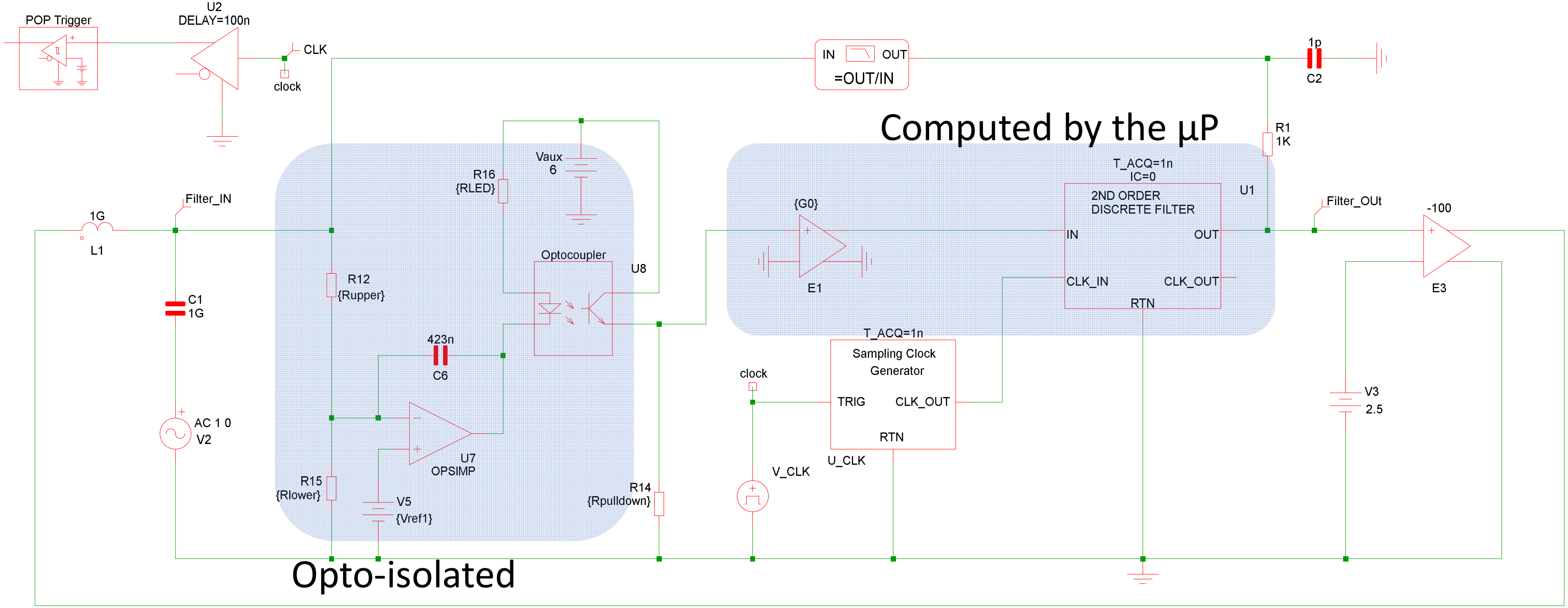
$$H(s)=\left(\frac{1+\dfrac{s}{\omega_z}}{1+\dfrac{s}{\omega_p}}\right)^2 \xrightarrow{\text{Bilinear transform}} H(z)=\frac{\omega_p{}^2\left(2z+T_s\omega_z+T_s\omega_z z-2\right)^2}{\omega_z{}^2\left(2z+T_s\omega_p+T_s\omega_p z-2\right)^2} \longrightarrow H(z)=\frac{a_0+a_1z^{-1}+a_2z^{-2}}{1+b_1z^{-1}+b_2z^{-2}}$$





Testing the Filter

- It is interesting to test the filter coefficients before going to code generation
- SIMPLIS offers a fast way for testing the front-end analogue part with the digital section

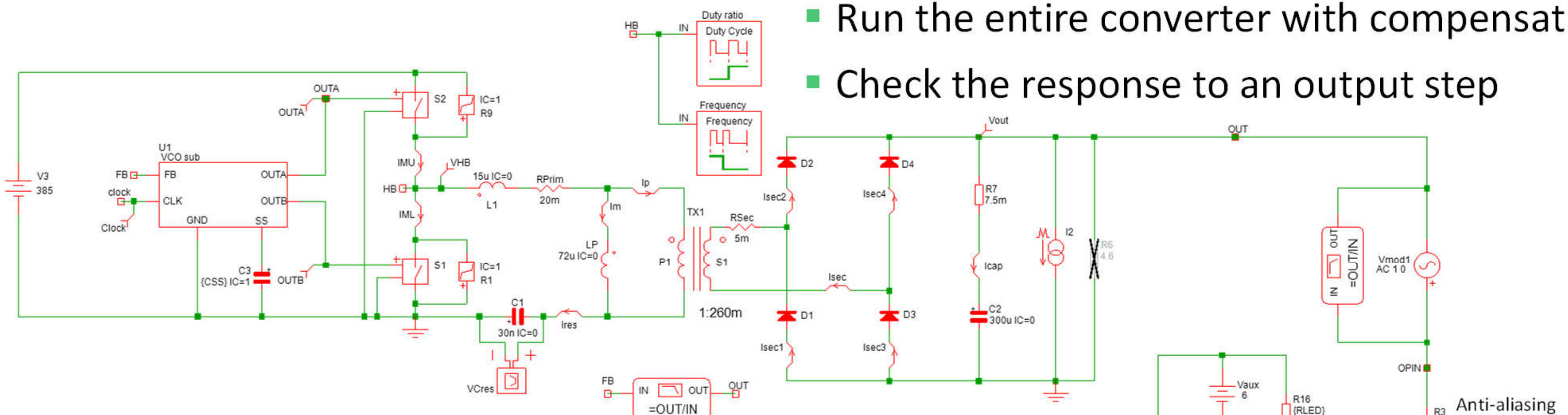


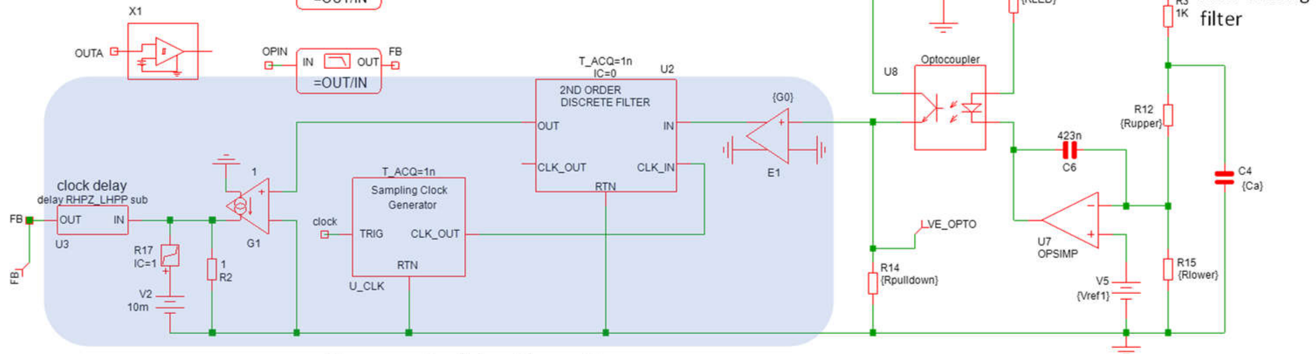
Computed by the µP

Opto-isolated secondary side

Simulating the Compensated Converter

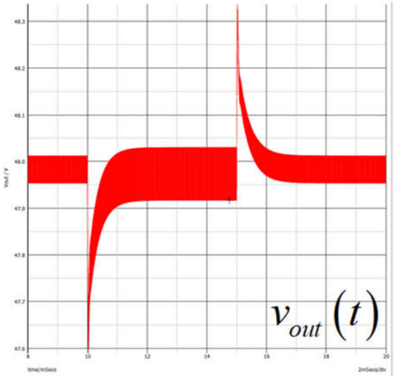
- Run the entire converter with compensation
- Check the response to an output step





Anti-aliasing filter

Computed by the µP



Output voltage response to the load step, V_{in} = 385 V

The Digital Filter – A modified PID

- It is also possible to adjust coefficients of an existing PID library
- The PID transfer function includes 1 pole at the origin and 2 zeroes

✓ Bring k_i to zero and you are left with a dc gain and a zero:

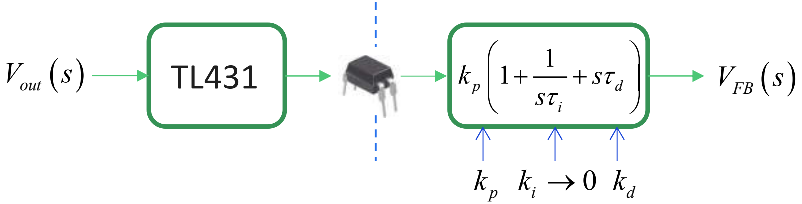
$$H_{PID}(s) = k_p\left(1+\boxed{\frac{1}{s\tau_i}}+s\tau_d\right)$$

Set it to 0

$$\Rightarrow \quad H_{PID}(s) = k_p\left(1+s\tau_d\right) = H_0\left(1+\frac{s}{\omega_z}\right)$$

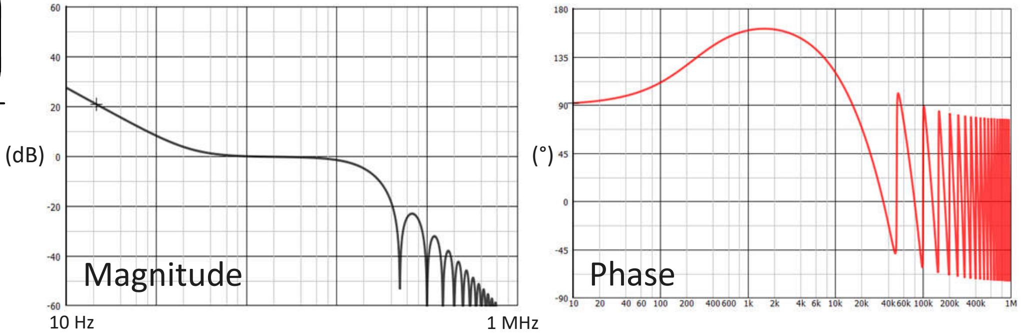
- Combined with the front-end analogue integrator, it breaks the -1-slope to 0:

$$\frac{V_{FB}(s)}{V_{out}(s)} = -\frac{R_{pulldown}\mathrm{CTR}}{R_{LED}}k_p\frac{\left(1+\frac{1}{sR_{upper}C_1}\right)\left(1+s\frac{k_d}{k_p}\right)}{1+sR_{pulldown}C_2}$$



$V_{out}(s)$ → TL431 → → $k_p\left(1+\frac{1}{s\tau_i}+s\tau_d\right)$ → $V_{FB}(s)$

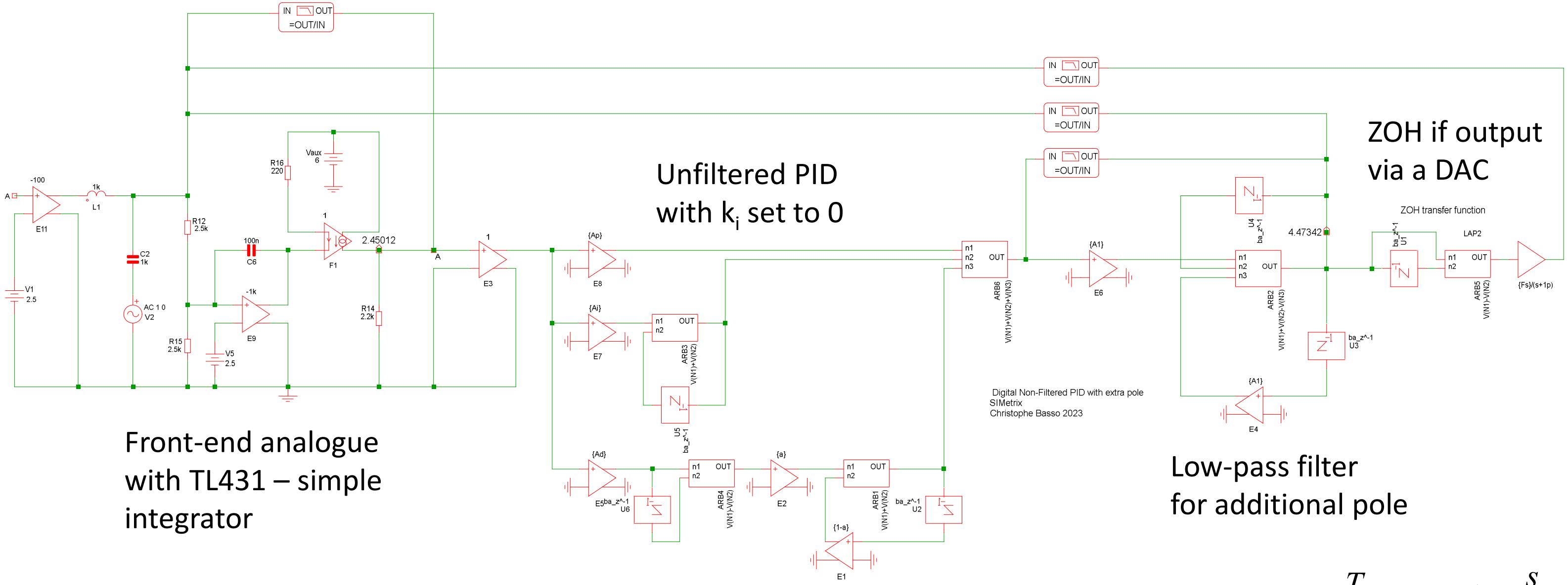
k_p $\quad k_i \to 0$ $\quad k_d$



This is a type 2 compensator

Final Implementation

- The original sampled PID is supplemented with a pole for filtering purpose
- The zero will be positioned before crossover for boosting the phase



Unfiltered PID with k_i set to 0

ZOH if output via a DAC

Front-end analogue with TL431 – simple integrator

Low-pass filter for additional pole

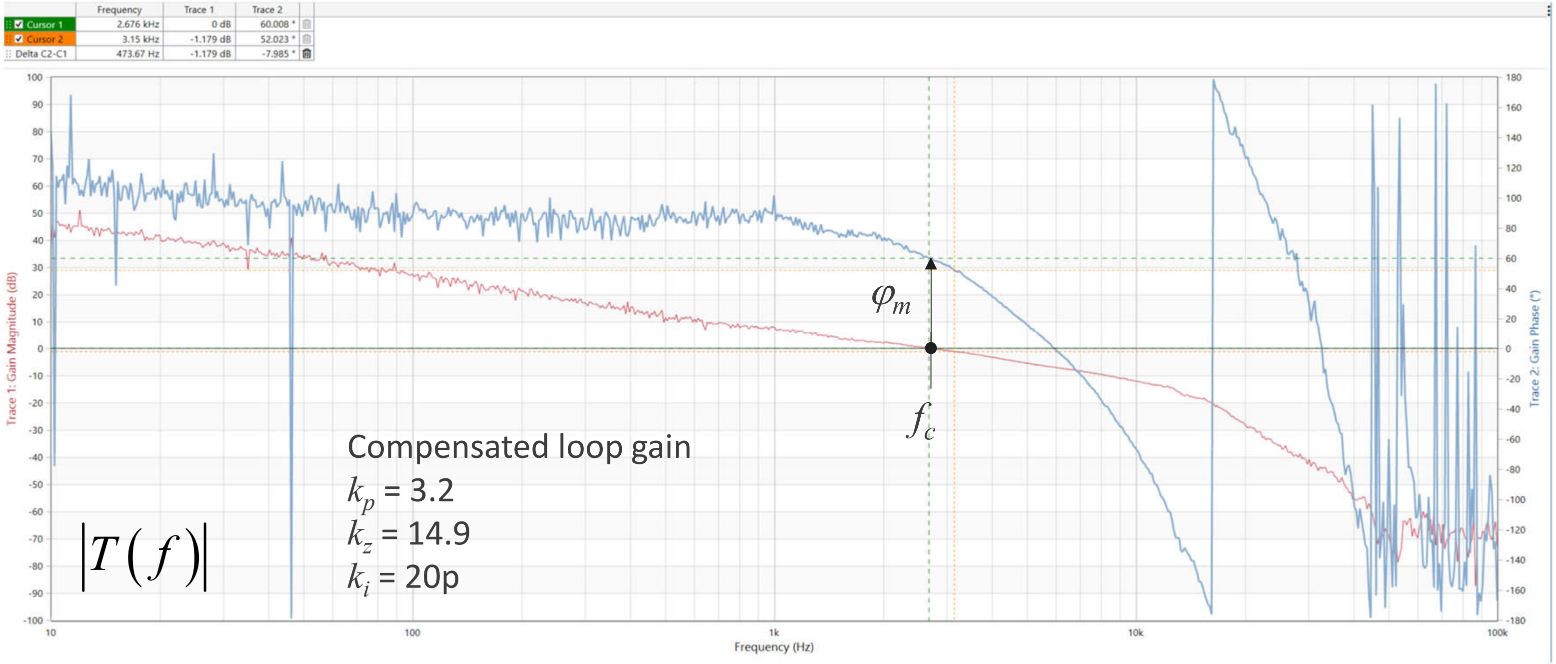
$$H_{TL431}(s) = \frac{\mathrm{CTR} \cdot R_{pulldown}}{R_{LED}} \cdot \frac{1}{\frac{s}{\omega_{po}}}$$

$$H_{PID}(s) = k_p\left(1 + \frac{1}{s\tau_i} + s\tau_d\right)$$

$$H_{LP}(s) = \frac{1 + s\frac{T_s}{2}}{1 + sT_s\left(2^n - \frac{1}{2}\right)} = \frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{\omega_p}}$$

Frequency Response

- A frequency-response analyzer (FRA) is used to graph the control-to-output response
- Crossover is set to 2.8 kHz and leads to a phase margin of 60°



	Frequency	Trace 1	Trace 2
☑ Cursor 1	2.676 kHz	0 dB	60.008 °
☑ Cursor 2	3.15 kHz	-1.179 dB	52.023 °
Delta C2-C1	473.67 Hz	-1.179 dB	-7.985 °

Compensated loop gain

k_p = 3.2

k_z = 14.9

k_i = 20p

Agenda

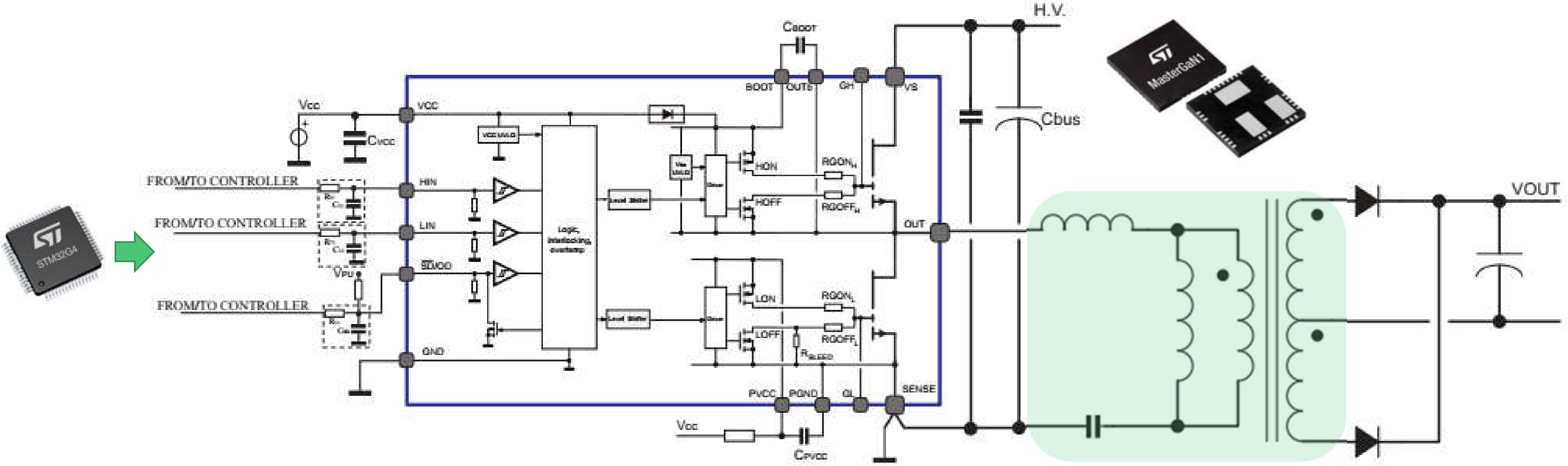
- The LLC Converter
- Controlling the Power Flow
- A Closed-Loop Control System
- Bringing a Microcontroller on Board
- Combining Analogue and Digital
- Practical Implementation
- Conclusion

High-Voltage Stage

- The half-bridge uses a MASTERGAN1 from ST which leads to a compact solution

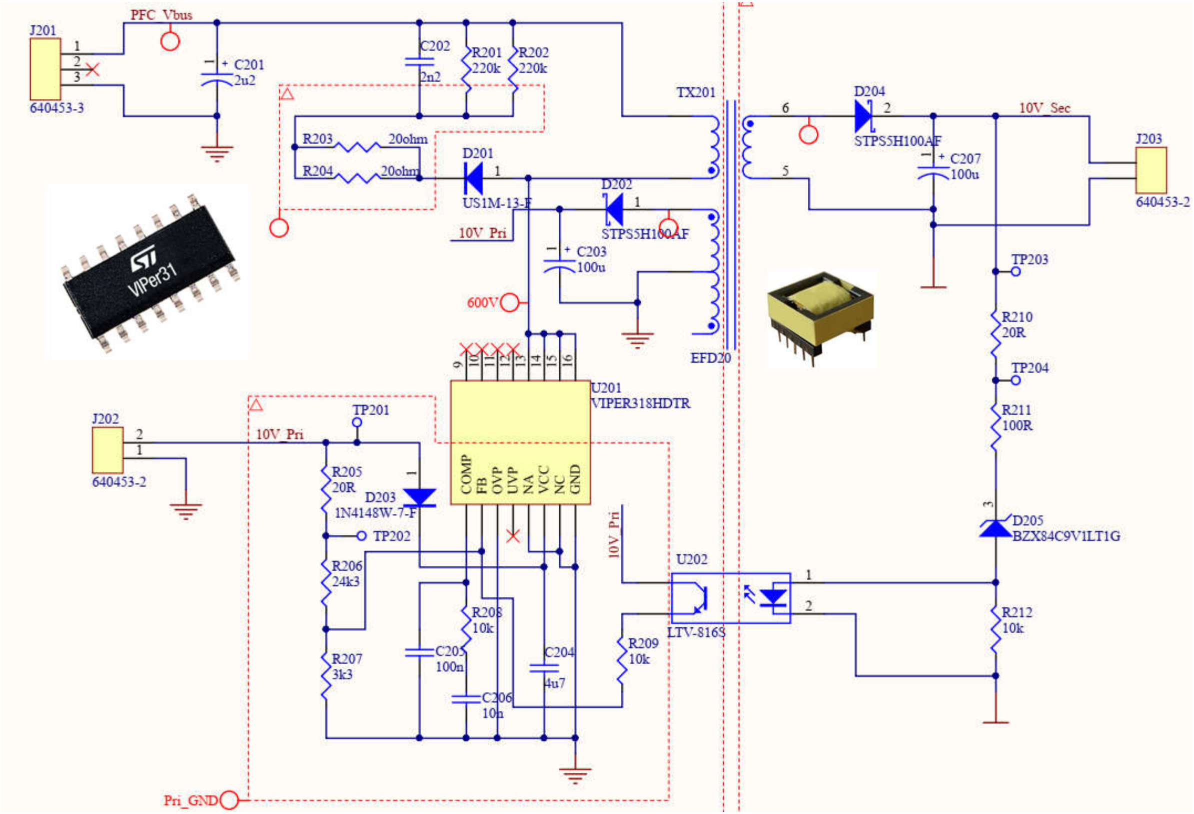
✓ 600-V 150-mΩ $r_{DS(on)}$ GaN transistors with onboard bootstrap diode

✓ Least components count when used in an LLC converter



LLC stage

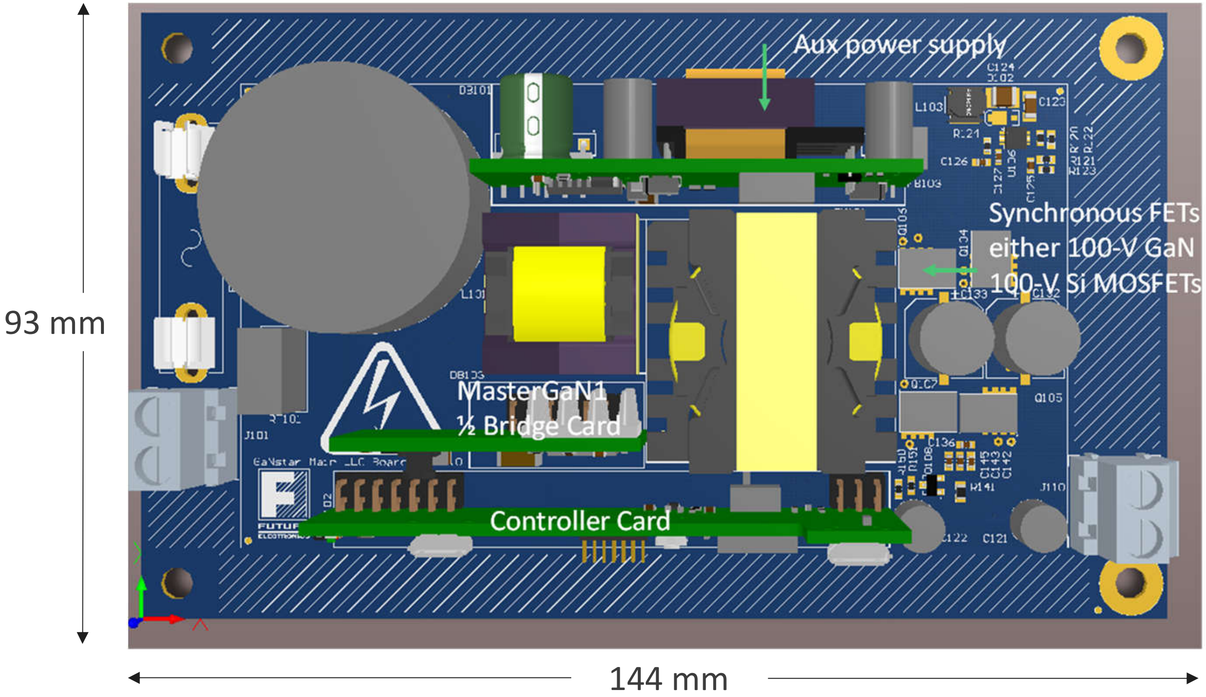
Auxiliary Power Supply



- The 10-V auxiliary power supply feeds the board and provides a voltage for:
  - ✓ Powering the STM32 micro-controller
  - ✓ Biasing the GaN drivers with a 5-V downstream dc-dc
- The flyback delivers a raw voltage whose value is set by a Zener-based loop.

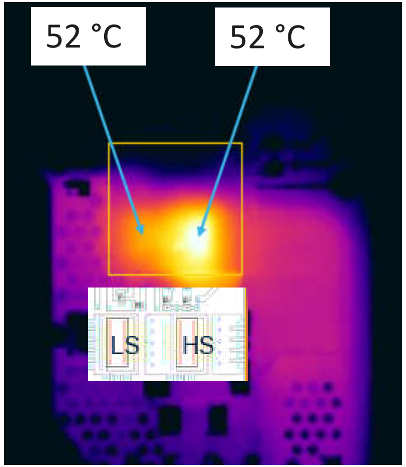
Practical Implementation

- The converter has been assembled in a compact format owing to integrated components
- ✓ A miniature fan has been added for a permanent 500-W power delivery



Thermal Performance

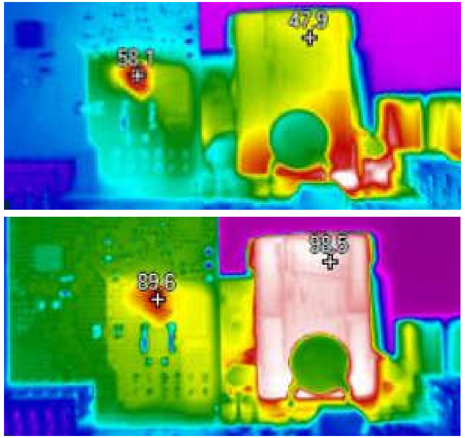
- Temperature measurements have been carried on the board with and without fan
- The losses on the MasterGaN half-bridge are kept within safe limits



The dissipated power is very well balanced between the low- and high-side transistors

The power is dissipated through the PCB vias and proper routing is essential to maximize the heat flow to the heatsink on the other side.

With fan, T_A = 25 °C



P_{out} = 500 W
T_{GaN} = 58 °C

P_{out} = 400 W
T_{GaN} = 90 °C

Without fan, T_A = 25 °C

The operating temperature remains in safe limits for a continuous 500-W power with a fan.

Conclusion and Future Work

- A microcontroller placed in the primary side requires an isolated image of V_{out} for regulating
- A fully-isolated amplifier represents an option but is not an option for cost reasons
- The literature reports regulation with a microcontroller based on a type 2 or 3 in the sec. side
- It defeats the possibility to implement a digital control loop in the microcontroller
- We propose an analogue integrator which transmits an isolated error signal to the primary side
- This analogue integrator is supplemented by a digitally-implemented compensation strategy
- Combining both approaches brings the low cost of the analogue option and the flexibility of digital coding.
- The next step is to control a PFC front-end stage with the microcontroller