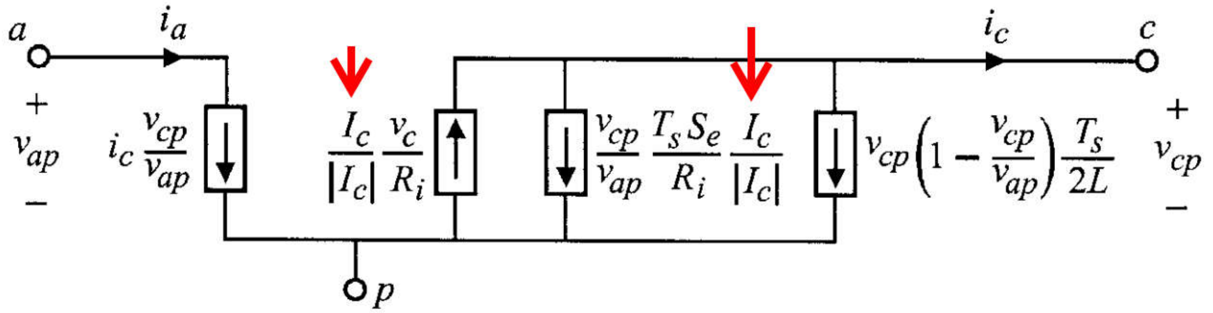
The PWM switch model introduced by Vatché Vorpérian in 1986 describes a way to model a voltage-mode switching converter with the VM-PWM switch model. The large-signal model is equivalent to a dc transformer whose turns ratio is D, the controlled duty ratio. Later, in 1990, Vatché published another model, the CM-PWM switch model, targetting peak current mode controlled converters. The model nicely predicts subharmonic oscillations and works in large-signal conditions: it can compute its bias point and it works in transient analysis. This current mode model was preceded by that developed by Ray Ridley using sampled data analysis. Ridley's model predicts the same dynamic response than what the CM-PWM switch does, but it only works in ac and cannot compute its bias point. The CM-PWM switch is sometimes prone to convergence problems and Vatché published a revised netlist in his 2004 book Fast Analytical Techniques for Electrical and Electronic Circuits. The fix is to add a coefficient in front of the two sources setting the peak and average values. It appears below:



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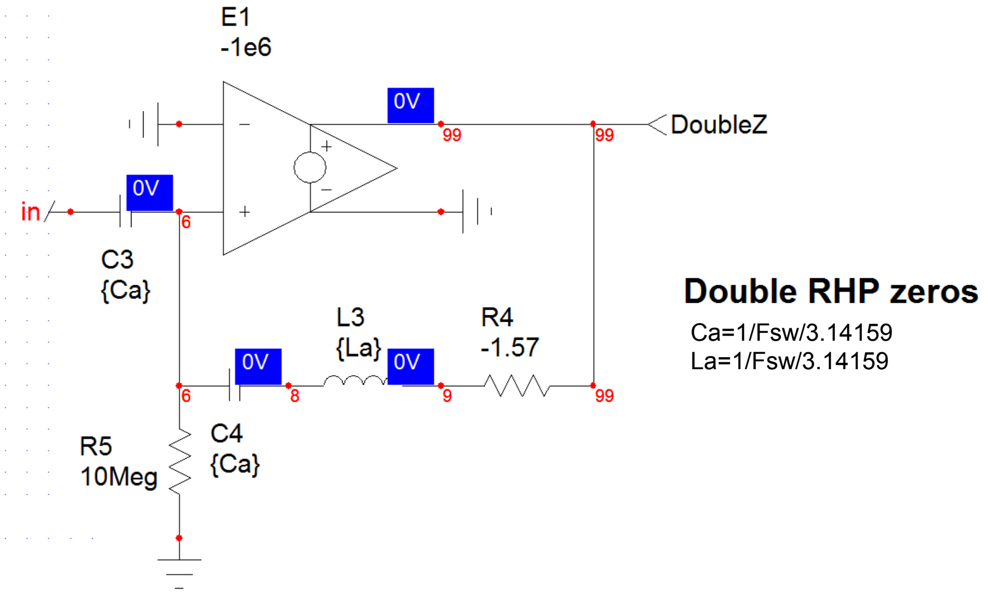
For some designers, the CC-PWM switch was troublesome given its difficulty – in some cases – to converge. The VM-PWM switch model is more robust and converges well. Ridley used the small-signal version of this VM-PWM switch to which he added a pair of RHP zeros to represent the sampling action in the current loop.



**Double RHP zeros**

Ca=1/Fsw/3.14159
La=1/Fsw/3.14159

This extra circuit uses a negative resistance value to produce a negative quality factor and thus RHP zeroes.

Rather than implementing a complex circuitry, the idea here is to reuse the classical VM-PWM switch and by adding a simple extra dummy source plus a capacitor, simulate the response of a current mode converter subject to subharmonic oscillations.

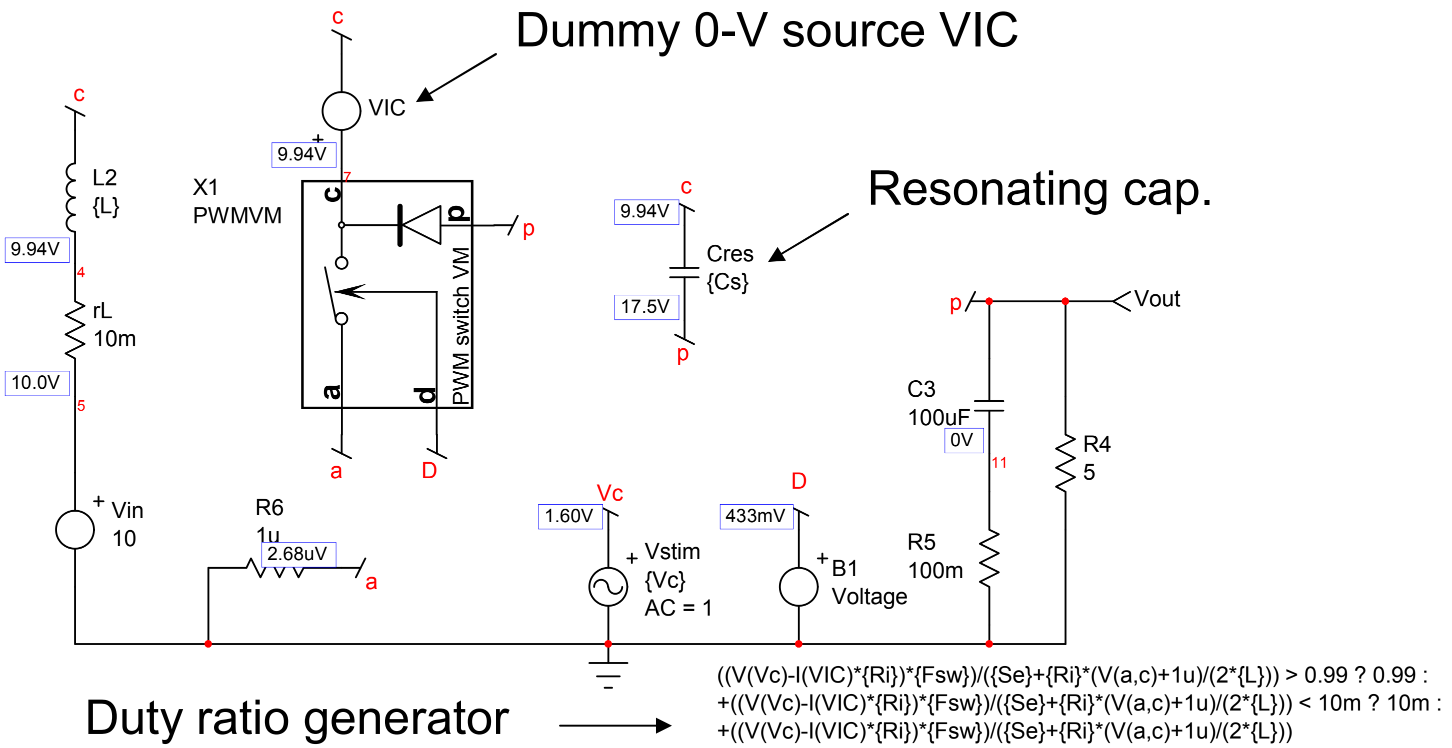
The implementation is very simple. Build a clamped source driving the duty ratio input of the PWM switch model. It is a voltage source clamped between 10 mV and 999 mV (1 to 99% duty ratio).

```
((V(Vc)-I(VIC)*{Ri})*{Fsw})/({Se}+{Ri}*(V(a,c)+1u)/(2*{L})) > 0.99 ? 0.99 :
+((V(Vc)-I(VIC)*{Ri})*{Fsw})/({Se}+{Ri}*(V(a,c)+1u)/(2*{L})) < 10m ? 10m :
+((V(Vc)-I(VIC)*{Ri})*{Fsw})/({Se}+{Ri}*(V(a,c)+1u)/(2*{L}))
```

It is actually the equation described in the book ***Switch-Mode Power Supplies: Spice Simulations and Practical Designs*** sec. ed. on page 199. Add a dummy voltage source in series with the c terminal that you call VIC plus a resonating capacitor between terminals c and p. The capacitor value is classically

```
Cs=1/(L*(Fsw*3.14)^2)
```

The control voltage $V_c$ is transformed into a duty ratio via the in-line equation to generate the correct duty ratio D. The following slide shows the final implementation around the VM-PWM switch model. This is a CCM simulation only here and I am not sure it would be easy to have the D generator toggle into a DCM expression easily.



Dummy 0-V source VIC

Resonating cap.

Duty ratio generator

((V(Vc)-I(VIC)*{Ri})*{Fsw})/({Se}+{Ri}*(V(a,c)+1u)/(2*{L})) > 0.99 ? 0.99 :
+((V(Vc)-I(VIC)*{Ri})*{Fsw})/({Se}+{Ri}*(V(a,c)+1u)/(2*{L})) < 10m ? 10m :
+((V(Vc)-I(VIC)*{Ri})*{Fsw})/({Se}+{Ri}*(V(a,c)+1u)/(2*{L}))

parameters

Fsw=100k
L=100u
Cs=1/(L*(Fsw*3.14)^2)
Ri=-250m
Se=0
Vc=1.6

**Clamped expression for the duty ratio expression in CCM current-mode:**

**((V(Vc)-I(VIC)*{Ri})*{Fsw})/({Se}+{Ri}*(V(a,c)+1u)/(2*{L})) > 0.99 ? 0.99 :**
**+((V(Vc)-I(VIC)*{Ri})*{Fsw})/({Se}+{Ri}*(V(a,c)+1u)/(2*{L}))**

This is a CCM current mode boost converter built around the voltage mode PWM switch model to which a duty ratio generator has been added, together with a resonating capacitor.

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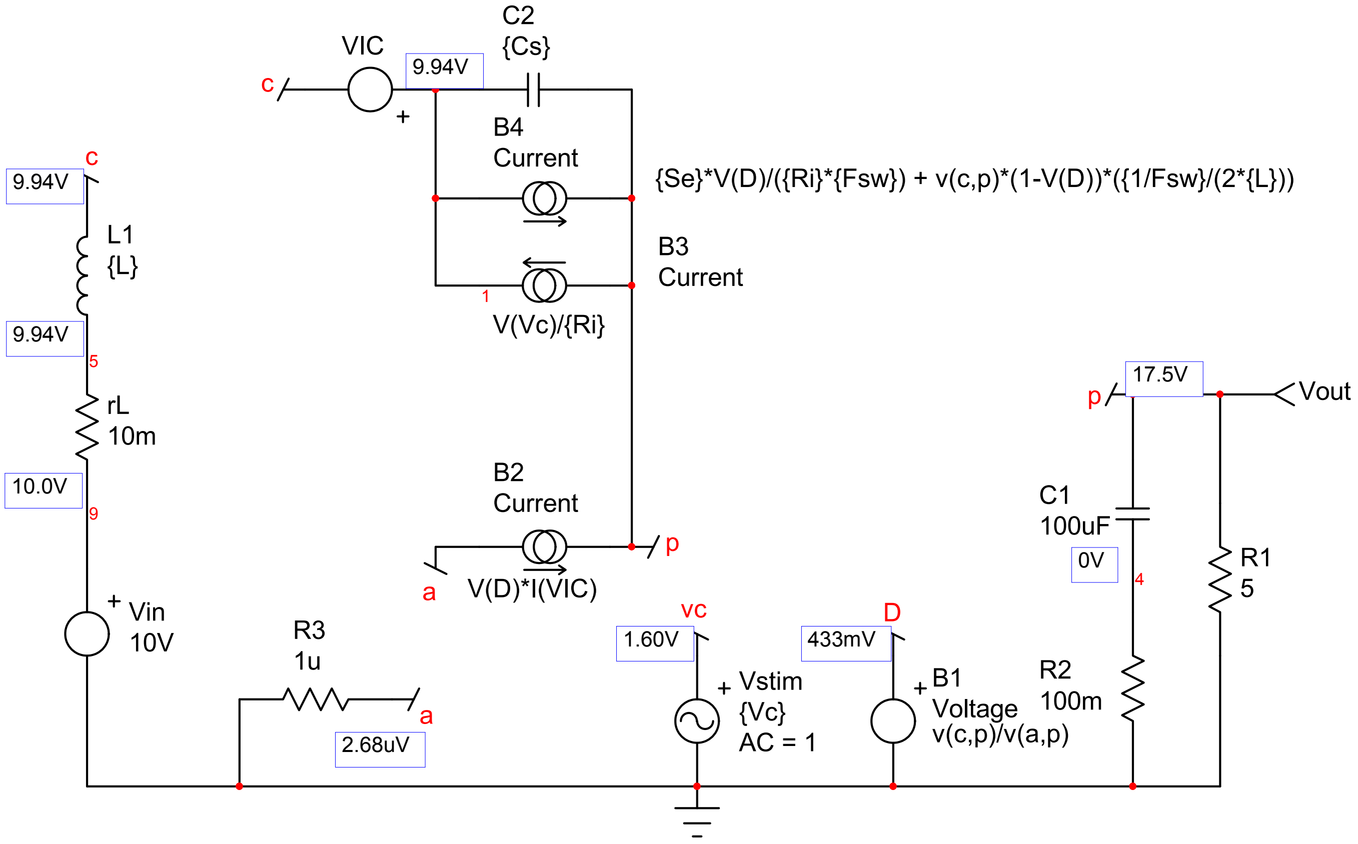
parameters

Fsw=100k
L=100u
Cs=1/(L*(Fsw*3.14)^2)
Ri=-250m
Se=0
Vc=1.6



This is the CCM current mode boost converter built around the original CM-PWM switch purposely thought to model current mode control power supplies. It only uses current sources. As you can see from the schematic, all operating points are similar to those from the previous slide.

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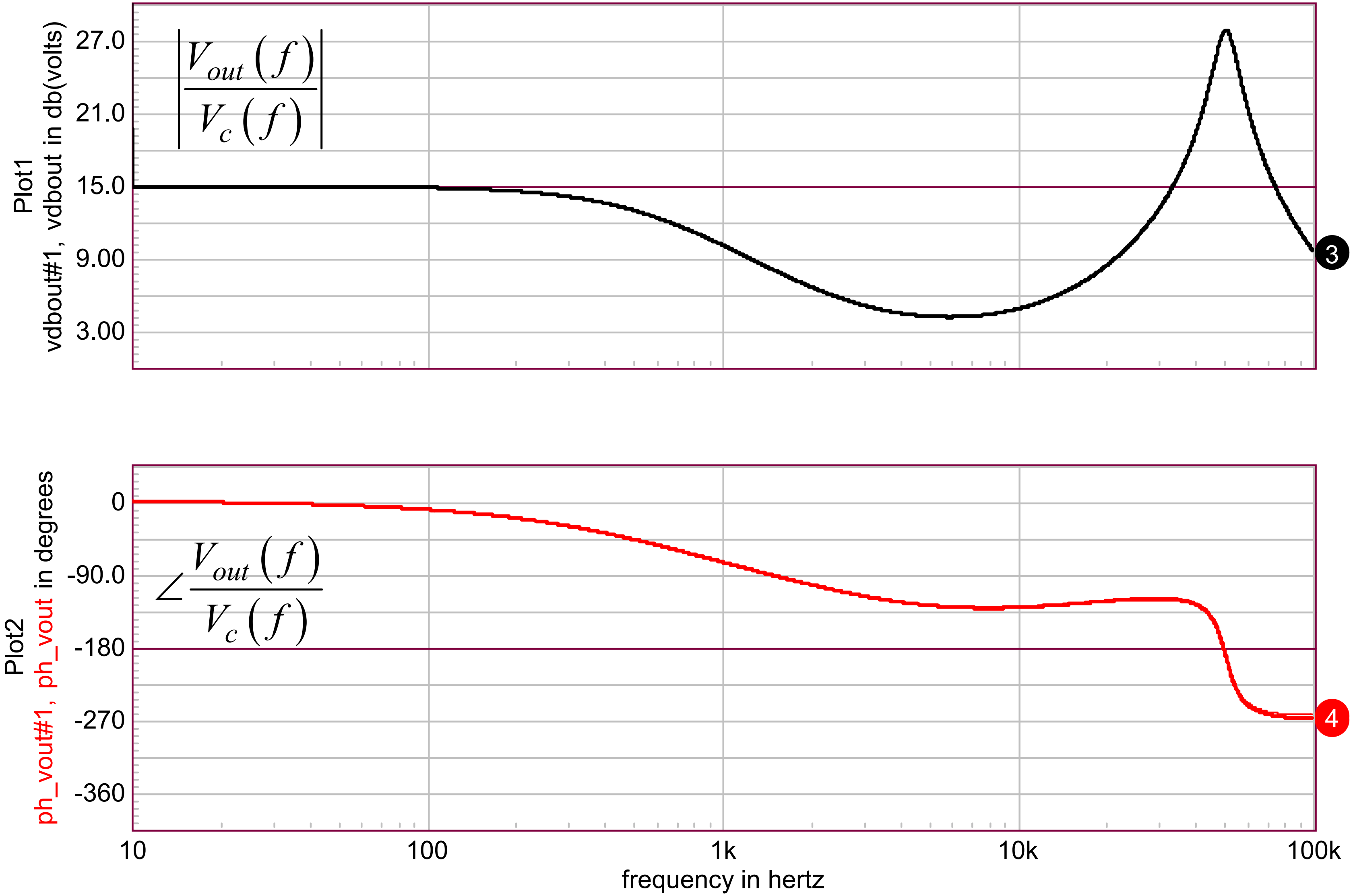
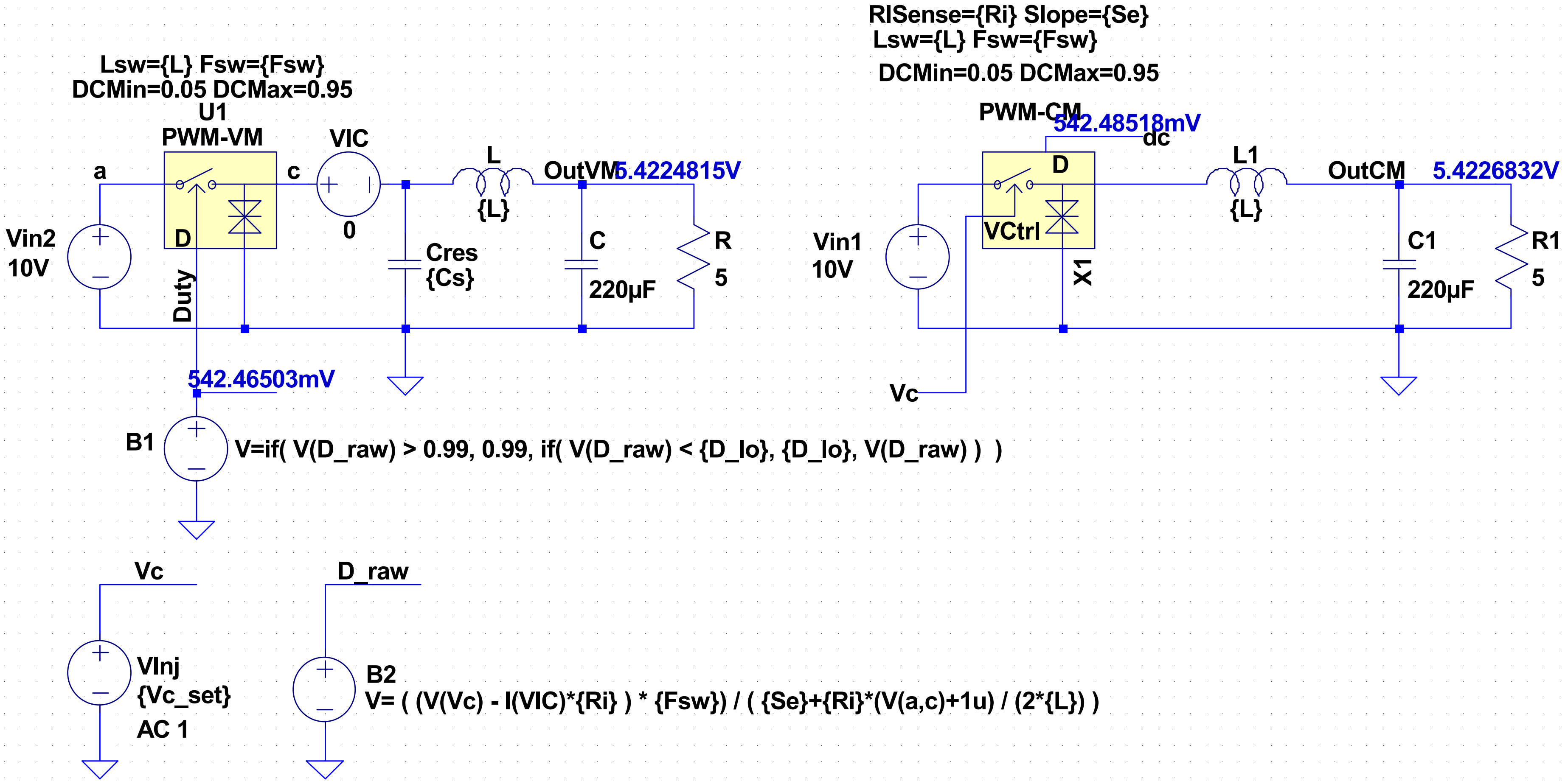
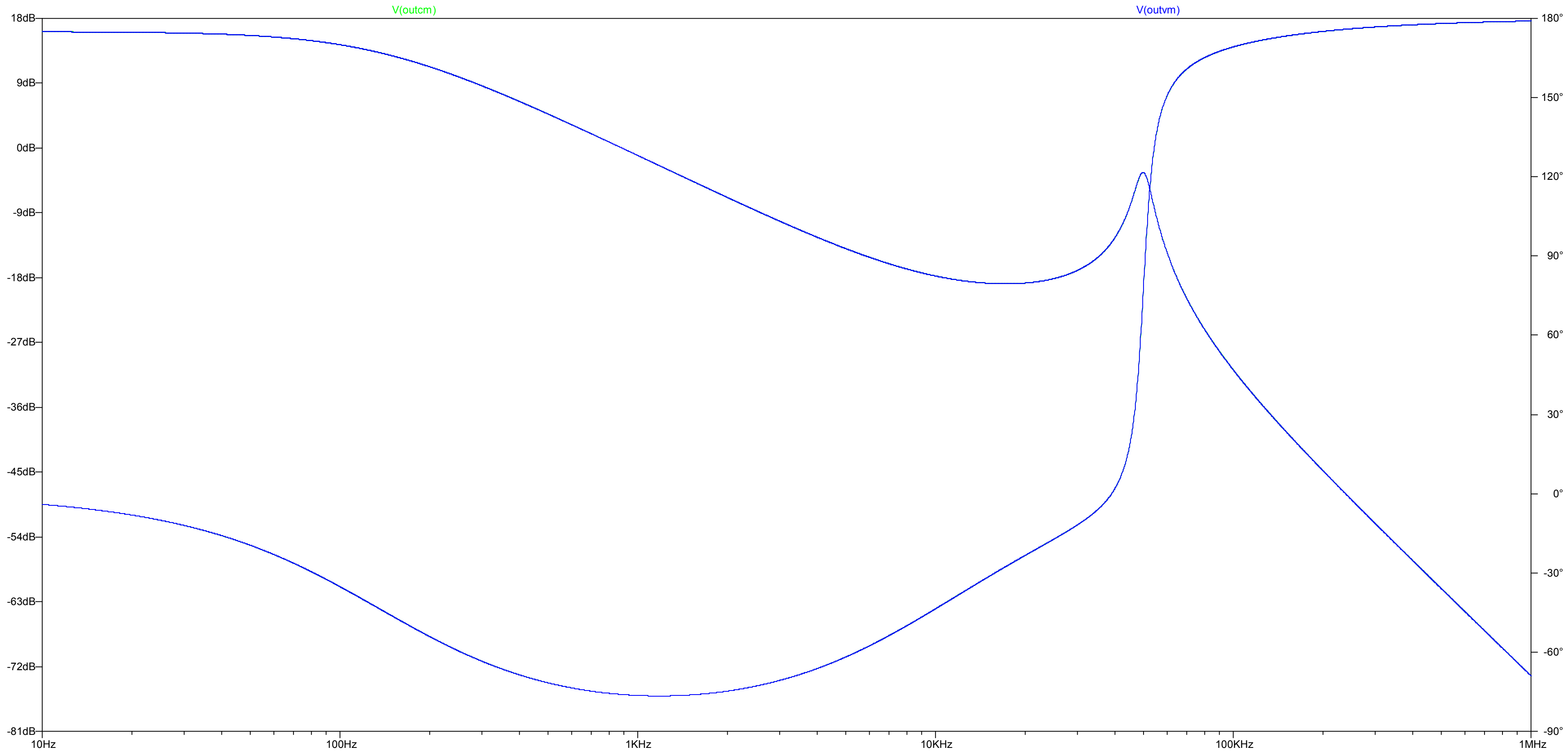


The graphs are well coincident and a small deviation appears as we approach $F_{sw}$ but it is reasonably low.



```
.Param L=75uH
.ac dec 1000 10 1000kHz
.param D_lo = 7u
.param D_hi = 0.99
.param Cs = {1/ ( L * (Fsw * 3.14)**2 ) }
.param Vc_set = 1
.param Fsw=100k
.param Ri=0.8
.param Se=0
```

Here in LTSpice, I compared a buck converter in CM driven by the VM-PWM switch model developped by Didier to which I added the resonating cap.



Dynamic responses from the VM-PWM switch with the added capacitor and the CM-PWM switch model. $F_{sw}$ = 100 kHz.

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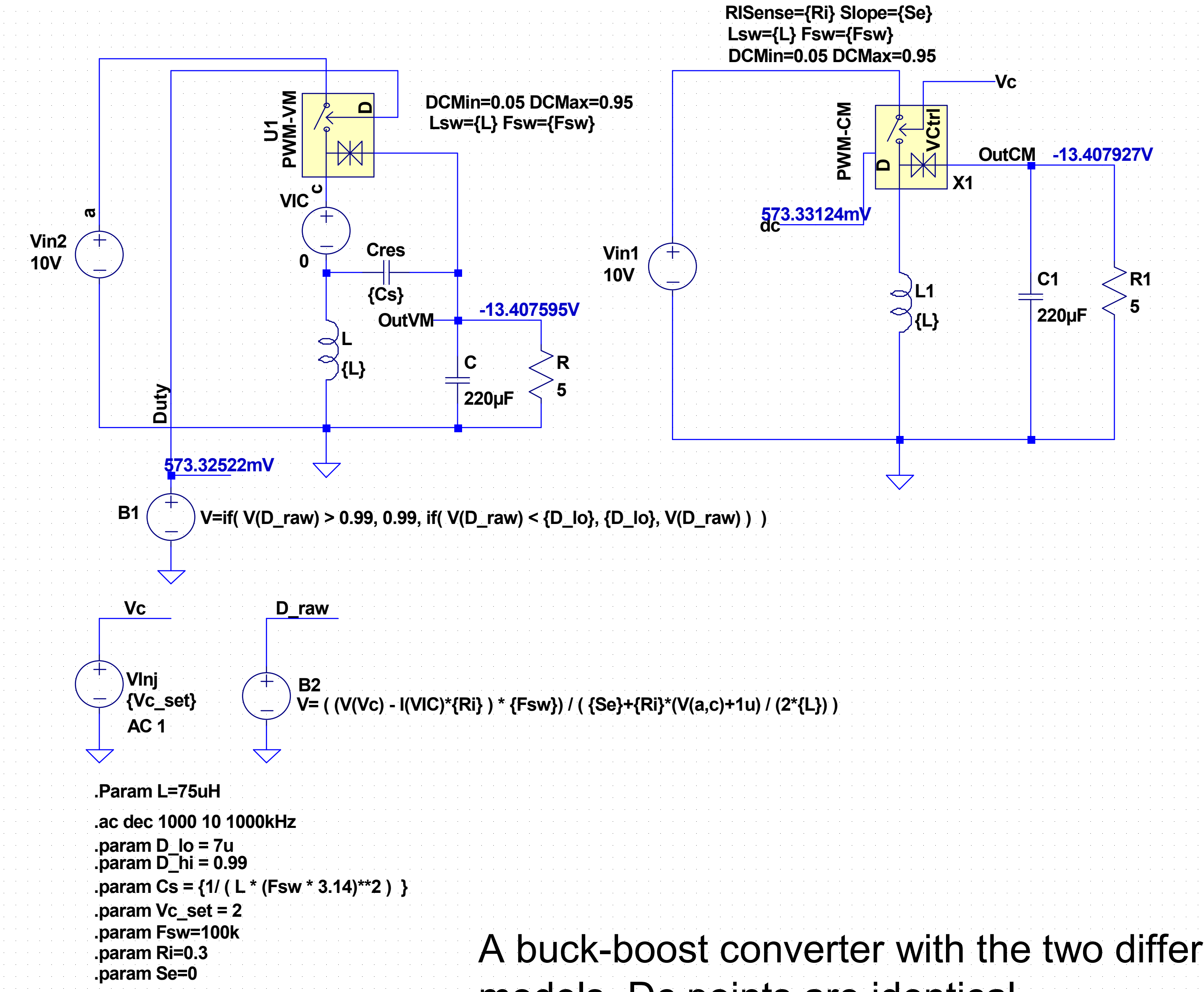

```
V=if( V(D_raw) > 0.99, 0.99, if( V(D_raw) < {D_lo}, {D_lo}, V(D_raw) )  )
V= ( (V(Vc) - I(VIC)*{Ri} ) * {Fsw}) / ( {Se}+{Ri}*(V(a,c)+1u) / (2*{L}) )
```

```
.Param L=75uH
.ac dec 1000 10 1000kHz
.param D_lo = 7u
.param D_hi = 0.99
.param Cs = {1/ ( L * (Fsw * 3.14)**2 )  }
.param Vc_set = 2
.param Fsw=100k
.param Ri=0.3
.param Se=0
```

A buck-boost converter with the two different models. Dc points are identical.

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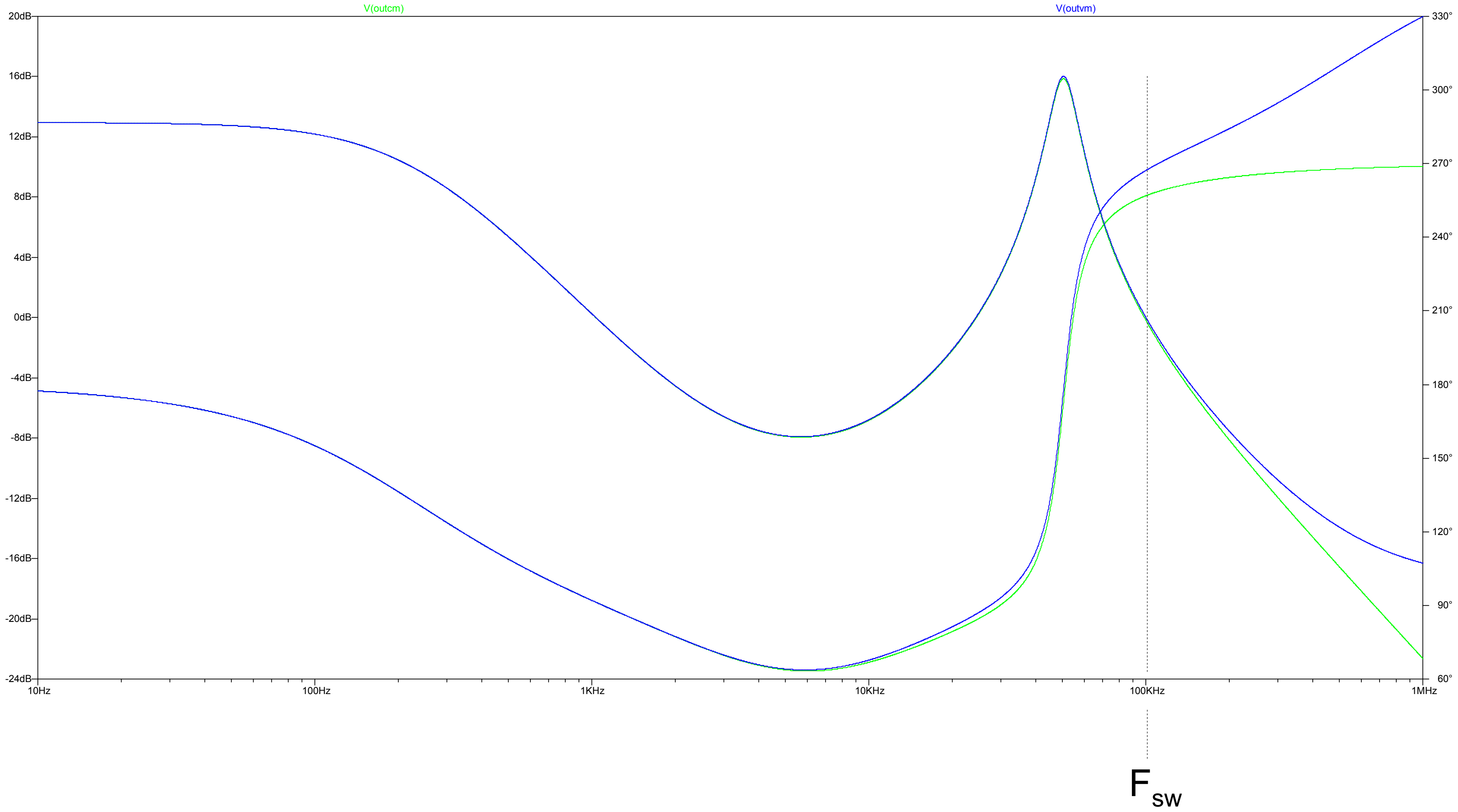

$F_{sw}$

Dynamic responses from the VM-PWM switch with the added capacitor and the CM-PWM switch model. $F_{sw}$ = 100 kHz.

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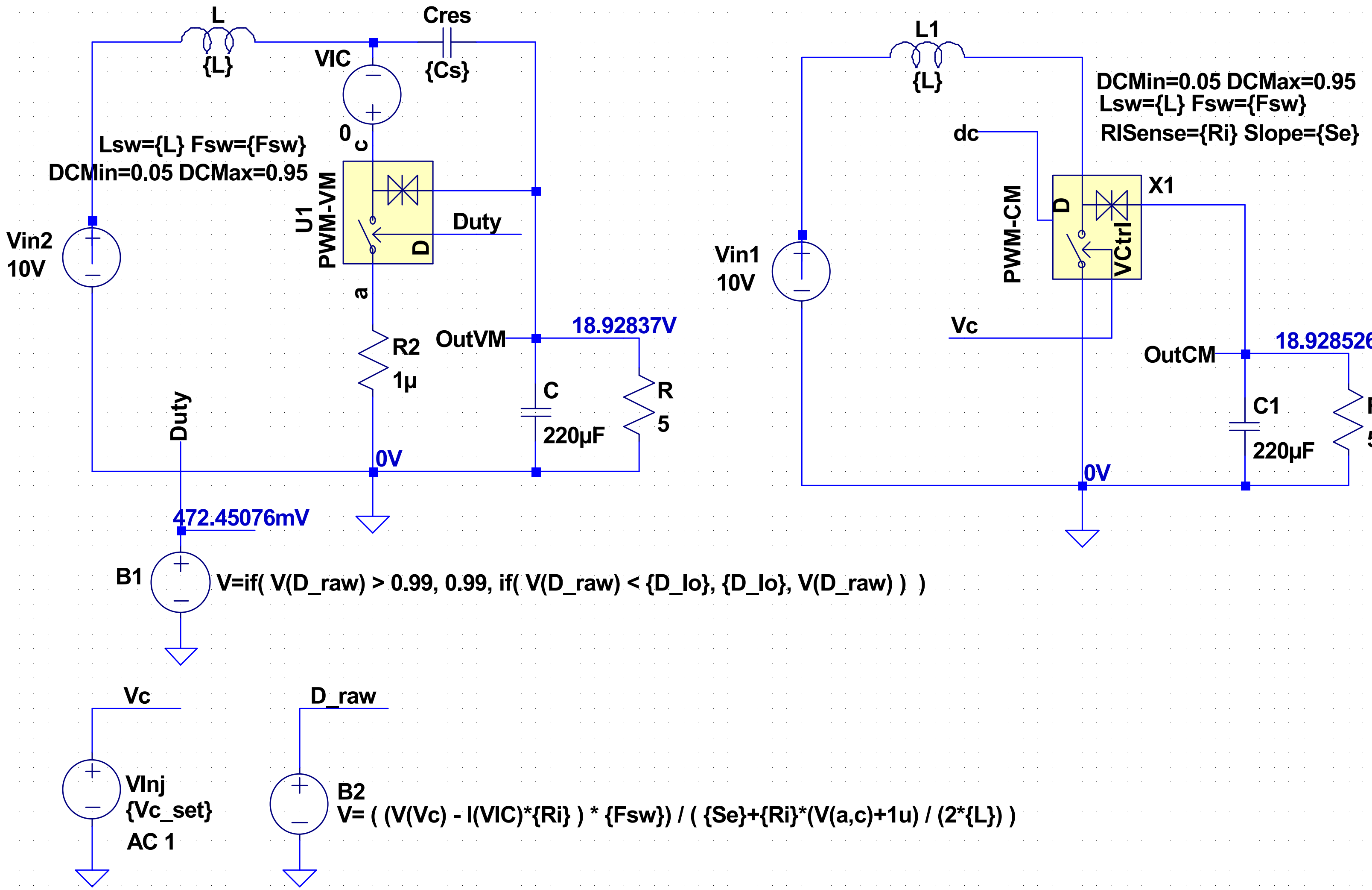

```
.Param L=50uH
.ac dec 1000 10 1000kHz
.param D_lo = 7u
.param D_hi = 0.99
.param Cs = {1/ ( L * (Fsw * 3.14)**2 ) }
.param Vc_set = 2.2
.param Fsw=300k
.param Ri=-0.3
.param Se=0
```

A boost converter with the two different models. Dc points are identical.

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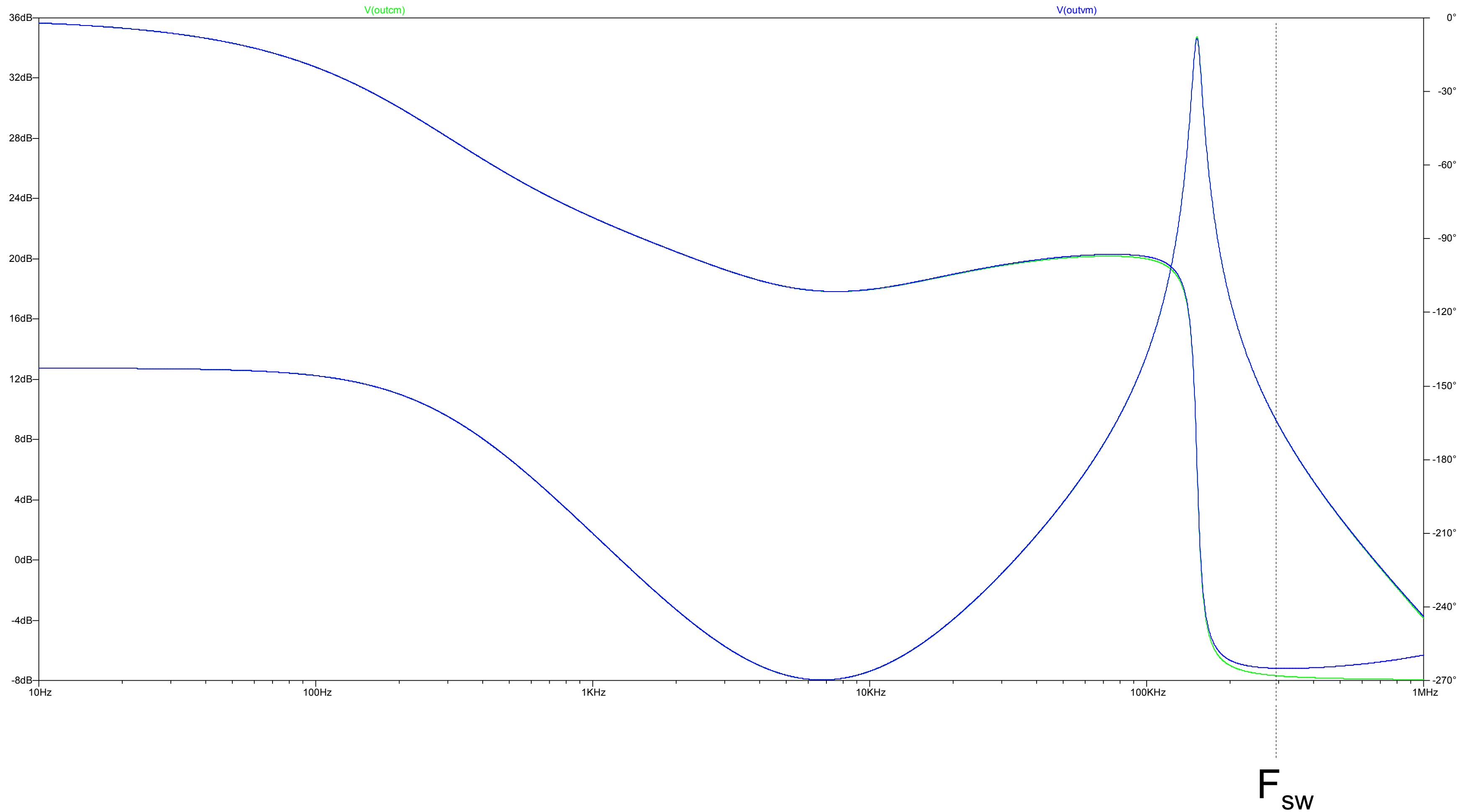

Dynamic responses from the VM-PWM switch with the added capacitor and the CM-PWM switch model. $F_{sw}$ = 300 kHz.

Special thanks to Marc Dimattina for helping me on this approach and of course to Didier Balocco for porting my models to LTSpice.

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