A Tutorial Introduction to Power Factor Correction

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Agenda

- Notions of Power Factor
- Power Factor Correction Structures
- Processing the Power
- Loop Compensation of a PFC
- Solutions from Future Suppliers
What is Power Factor?

- The goal of any power factor correction circuit is to emulate a resistance.
- The absorbed current must be sinusoidal and in phase with the input voltage.

\[ P_{in} (t) = I_{in} (t) \cdot V_{in} (t) = \frac{V_{in} (t)}{R} \]

\[ P_{in,avg} = \frac{1}{T_{line}} \int_0^{T_{line}} p_{in}(t) \cdot dt = 70 \text{ W} \]

\[ P_{in,app} = V_{in,\text{rms}} \cdot I_{in,\text{rms}} = 85 \times 823 \text{ m} = 70 \text{ VA} \]

\[ \text{PF} = \frac{\text{active power \ [W]}}{\text{apparent power \ [V \cdot A]}} = 1 \]

\[ P_{in,avg} = \frac{1}{T_{line}} \int_0^{T_{line}} p_{in}(t) \cdot dt = 70 \text{ W} \]

\[ P_{in,app} = V_{in,\text{rms}} \cdot I_{in,\text{rms}} = 85 \times 1.46 = 124 \text{ VA} \]

\[ \text{PF} = \frac{\text{active power \ [W]}}{\text{apparent power \ [V \cdot A]}} = 0.56 \]
What is the Impact of a Low PF?

- Assume a 250-W load absorbed by an equipment from a 110-V 15-A ac outlet
- With a PF of 0.56, the current is $250/110/0.56 = 4 \text{ A rms}$

✓ You can safely connect a maximum of 3 devices ($15/4 = 3.75$)

- Add a front-end power factor correction stage to bring PF close to unity

✓ You can safely connect 6 workstations
Explaining Power Factor with Beer

- A low power factor will force the circulation of a higher rms current
- Electric wires can overheat and utility companies push for power factor correction
- A glass of beer with an excessive foam can help appreciate the issue

![Diagram showing real power, apparent power, reactive power, and the relationship between them.]

**Equation:**

\[
S = P + jQ
\]

\[
Q = P \sqrt{1 - PF^2}
\]

If \( PF < 0.95 \),

\[
Q [VAR] > 33\% \cdot P [W]
\]

[Link to information page about reactive power on Iberdrola's website](https://www.iberdrola.es/en/homeowners-associations/information/reactive-power)
Power Factor and Distortion

- Power factor depends on two parameters:
  \[ \text{PF} = \left( \frac{I_{1,\text{rms}}}{I_{\text{rms}}} \cos \varphi \right) = k_d k_{\varphi} \]

  - \( k_d \): Represents the distortion factor
  - \( k_{\varphi} \): Designates the displacement angle

  \[ k_d < 1, \quad k_{\varphi} < 1 \]
  \[ k_d = 1, \quad k_{\varphi} < 1 \]
  \[ k_d = 1, \quad k_{\varphi} = 1 \]

  \( \text{PF} = \sqrt{1 + \left( \frac{\text{THD}}{100} \right)^2} \)

  - \( \text{THD} = 30\%, \, \text{PF} = 0.958 \)
  - \( \text{THD} = 10\%, \, \text{PF} = 0.995 \)
  - \( \text{THD} = 5\%, \, \text{PF} = 0.999 \)

  Check harmonics limits according to IEC1000-3-2
Equipment Compliance

- The standard EN61000-3-2 defines the class of equipment and associated limits

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<tr>
<td>P_in &gt; 75 W</td>
<td>P_in &gt; 75 W</td>
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NORME INTERNATIONALE INTERNATIONAL STANDARD

CEI IEC 61000-3-2
Deuxième édition Second edition 2000-08

Class D limits

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<th>Rang harmonique</th>
<th>Courant harmonique maximal autorisé par watt mA/W</th>
<th>Courant harmonique maximal autorisé A</th>
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<tr>
<td>11</td>
<td>0,35</td>
<td>0,33</td>
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<tr>
<td>13 ≤ n ≤ 39</td>
<td>n = 3,85 (harmoniques impairs seulement)</td>
<td>Voir tableau 1</td>
</tr>
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</table>
The Need for Storage

- The goal of a PFC front-end converter is to emulate a resistive load.
- The power of a single-phase ac source feeding a resistance involves a squared sinewave.

\[ P_{in} = 150 \text{ W} \]

\[ p_{in}(t) = v_{in}(t) \cdot i_{in}(t) \]

- Active power factor stores and release energy.

Store energy

Release energy

Output capacitor

\( v_{in}(t) \)

\( v_{out}(t) \)

\( F = 100 \text{ Hz} \)

\( (W) \)

\( (ms) \)

\( 0 \)

\( 10 \)

\( 20 \)

\( 30 \)

\( 40 \)

\( F = 50 \text{ Hz} \)

\( F = 100 \text{ Hz} \)

Output voltage ripple is twice the input frequency.

\( 420 \text{ V} \)

\( 400 \text{ V} \)

\( 380 \text{ V} \)

\( \langle p_{in}(t) \rangle = 150 \text{ W} \)

Power excess

Power shortage

\( P_{in} = 150 \text{ W} \)

\( 0 \)

\( 10 \)

\( 20 \)

\( 30 \)

\( 40 \)
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Passive Power Factor Correction

- Capacitor refueling in a full-bridge rectifier is confined at the sinewave peak
- A very narrow spike is generated, rich of numerous harmonics
- Spreading the current across the sinewave smooths the current signature

- Choke is bulky, heavy and induces mechanical stress
- Reduces rms current but marginal results harmonic-wise

\[
L_1 = 34 \text{ mH}
\]

\[
P_{out} = 100 \text{ W}
\]

\[
I_{in,\text{rms}} = 1.8 \text{ A} \quad \text{without } L
\]

\[
I_{in,\text{rms}} = 1.2 \text{ A} \quad \text{with } L = 34 \text{ mH}
\]
Active Power Factor Correction

- An active PFC forces a sinusoidal current absorption in phase with the voltage.

- A boost converter is traditionally employed for this operation.

\[ v_{rec}(t) \]

\[ i_{in}(t) \]

\[ L \]

\[ L \]

\[ i_{L}(t) \]

\[ i_{d}(t) \]

\[ i_{SW}(t) \]

\[ C_{bulk} \]

\[ R_L \]

\[ v_{out}(t) \]

100- or 120-Hz ripple

\[ 400 \text{ V} \]

- The rectified input voltage sets the inductor current envelope.

- The inductor current is adjusted to match power demand.
Conduction Mode – BCM or CrM

- Inductor current reduces to 0 A before a new cycle starts in borderline conduction mode
- Well suited for power levels up to 300 W or higher with interleaved version
- Near-zero-voltage switching in some conditions
- Discontinuous operation reduces $t_{rr}$-related power dissipation on the diode

- Variable-frequency switching makes light-load operation less efficient
- Internal frequency clamp or foldback is generally implemented to reduce losses
- Large circulating currents inducing conduction (rms) and core losses ($\Delta I_L$)
Conduction Mode - CCM

- The inductor current never touches zero within a switching cycle
  - Continuous conduction mode is well suited for high-power converters > 300 W
  - Current can be monitored by an independent loop for best distortion figures
  - Circulating rms currents are minimized with a moderately-low ripple current

- CCM induces switching losses and low-$t_{rr}$ diodes or SiC types are mandatory
- Larger inductance value compared to BCM operation
- Two loops to stabilize in the classical multiplier-based approach
Single-Stage Converters

- It is possible to combine a PFC stage with an isolated flyback converter
- This single-stage approach is well adapted to power levels up to 100-150 W
- The components count is reduced
- It provides galvanic isolation to the downstream load
- Large output capacitance for the storing process
- Fairly-distorted input current barely passes PF specifications
- Slow-loop operation makes it well suited for lighting systems
Bridgeless PFC

- The bridge hampers overall efficiency with two permanently-conducting diodes

\[ P_d \approx 2V_f I_{d,\text{avg}} \]

\[ I_{F,\text{avg}} = \frac{2 \sqrt{2P_{\text{out}}}}{\pi V_{ac,LL} \eta} \]

\[ P = 300 \text{ W} \quad \eta = 100\% \]

\[ V_{ac,LL} = 90 \text{ V rms} \]

\[ P_d \approx 5 \text{ W} \]

Eff. loss \( \approx 1.7\% \)

- The bridgeless PFC ensures one diode conduction via the MOSFET body

- **Only one diode is conducting in low frequency**

- **The MOSFETs share a common drive signal without caring about line polarity**

- **Poor common-mode noise signature**

---

Variation of the Bridgeless PFC

- The original scheme suffers from a poor common-mode EMI signature
- A variation around this circuit was proposed by Ivo Barbi in 1999

- Two PFC in parallel driven by the same pattern – easy to drive with one controller
- Conventional structure automatically activated depending on the line polarity

A. F. de Souza and I. Barbi, High power factor rectifier with reduced conduction and commutation losses, 21st International Telecommunications Energy Conference. INTELEC '99 (Cat. No.99CH37007), 1999
The Totem-Pole PFC

- The two high-frequency switches are connected in a half-bridge configuration
- Two diodes in the slow leg route the low-frequency portion of the input current

![Diagram of the Totem-Pole PFC]

- The fast-leg transistors alternatively perform as power switch and catch diode
- $D_2$ and $D_1$ must be fast diodes with no recovery loss: SiC or GaN transistors are perfect for this function
- $D_3$ and $D_4$ can be controlled-switches for improved efficiency
- Common-mode noise improved compared to bridgeless PFC
The Need to Detect the Input Line Polarity

- Each fast-leg transistor alternatively plays the role of the switch and the diode
- The switching element needs instruction on the input line polarity

Manage line polarity
Dedicated Controllers for TPPFC

- **onsemi** has introduced two low-voltage controllers operating in BCM and CCM
- NCP1680 can implement a pre-converter up to 300 W

- One single inductor with auxiliary winding ensures ZVS operation
- Line management with a pair of resistive dividers
- Two external drivers dedicated to fast and slow legs: NCP51820 and NCP51530
Efficiency Performance of the BCM TPPFC

- The TPPFC efficiency is excellent compared with a classical approach
- A gain of 1.8% is brought by the all-synchronous approach at 90-V rms input voltage

Efficiency approaches 99% at 230 V rms and full power
TPPFC High-Power Operations

- Continuous conduction mode is selected for high-power PFC pre-converters
- The NCP1681 includes a multi-mode engine operating in CCM, BCM and DCM
- Mode change is inhibited for high-power applications and the part keeps CCM
Multi-Mode Operations

- The downstream converter may operate with different load profiles, low to high current
- CCM is optimized for high power but BCM and DCM bring better efficiency at lighter loads
- NCP1681 embarks a multi-mode engine smoothly transitioning across all these modes

The part internally compares operating timings with thresholds to determine the mode
The mode is kept during an entire half cycle
Managing Current Transformers

- Fast-leg switches play the main power switch or the rectifier role in a TPPFC
- Current flow in the leg depends on the input line polarity and needs specific action
  - Current transformers secondaries are alternatively shorted depending on line polarity
A Reliable Controller with Fault Management

- The controller permanently monitors operating variables for maximum protection
- Some minor faults involve a quick recovery while heavier issues start a 500-ms timer

<table>
<thead>
<tr>
<th>Fault</th>
<th>Trigger</th>
<th>Cleared By*</th>
<th>Comments / Notes</th>
</tr>
</thead>
</table>
| UVP          | $V_{FB} < V_{UVP}$       | $V_{FB} > V_{UVP} + V_{UVP(HYS)}$ | - All DRV pulses are stopped
- PFC_OK signal pulled to GND
- Polarity signal remains ON

| BUV (Bulk Under-Voltage) | $V_{FB} < V_{BUV} + PFC_OK$ | $T_{BUV}$ expires         | - BUV stops DRV (Soft-stop option)
- PFC_OK signal pulled to GND.
- Polarity signal remains on
- 500 ms restart timer

| Soft OVP      | $V_{FB} > V_{softOVP}$    | $V_{FB} < V_{OVPRecover}$ | - Fast leg DRV's disabled if soft OVP sequence completes
- All other signals remain active
- Soft start on recovery |

| Hard OVP      | $V_{FB} > V_{hardOVP}$    | $V_{FB} < V_{OVPRecover}$ | - Fast DRV pulses are stopped immediately
- Polarity remains on
- Slow leg and open loop drive signals remain ON
- Soft start on recovery |

- ✓ UVP or under-voltage protection monitors the FB pin and checks for a bias before delivering pulses
- ✓ BUV or bulk under-voltage checks that the output voltage is above 80% of its nominal value
- ✓ Soft OVP is active when a benign overshoot is detected like a load release
- ✓ Hard OVP can be seen as more severe fault in case of stronger overshoot or loop failure
NCP1681 Evaluation Board

- A 500-W demonstration board operated in multi-mode

Optional in-rush limiter

By-pass diodes

CT blanking

To upper fast-leg

Slow-leg
The Control Section

- The NCP1681 senses the polarity via two resistive networks.
- The slow-leg requires a bootstrapped driver but of lesser speed than for GaNs.

Feedback connection for regulation and BUV.

Zero crossing detection for inductor current downslope.

Input mains polarity detection.

Polarity indicator for CT short.

Slow-leg control signal.

To GaNs.

V_{cc} OVP and OTP.

To SJ MOSFETs.

Feedback connection for regulation and BUV.

√ One option with isolated gate driver NCP51561 and discrete GaNs (GS66508B).

√ One option with one NCP51561 and two NCP58921.
NCP51561 Half-Bridge Driver

- Isolated drivers are preferred for the fast leg considering switching speed and noise
- Differential voltage up to 1.5 kV between channels
- 5-ns delay matching and pulse distortion
- Common Mode Transient Immunity greater than 200 V/ns
NCP58921 Integrated GaN Driver

- Integrated GaN and driver simplifies PCB layout and reduces BOM cost
Efficiency Charts with Multi-Mode Engine

- The multi-mode engines clearly show its positive effects in light-load conditions
Operating Waveforms

- The part excels in distortion performance which keeps below 5% at full load.

\[ V_{\text{in}} = 115 \text{ V rms} - \text{THD} = 4.2\% \]

\[ V_{\text{in}} = 230 \text{ V rms} - \text{THD} = 2.7\% \]
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- Loop Compensation of a PFC
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Constant On-Time Control

- Voltage-mode control offers the easiest implementation for BCM PFCs.

- Start with the inductor instantaneous current waveform:

\[
i_L(t) = \frac{I_{\text{peak}}}{2}
\]

- The power sets the on-time value in relationship with the rms input voltage:

\[
p_{\text{in}}(t) = v_{\text{in}}(t)i_{\text{in}}(t) = v_{\text{in}}(t)\frac{i_{L,\text{peak}}(t)}{2}
\]

\[
i_{L,\text{peak}}(t) = \frac{v_{\text{in}}(t)}{L}t_{\text{on}}(t)
\]

\[
p_{\text{in}}(t) = \frac{v_{\text{in}}^2(t)}{2L}t_{\text{on}}(t)
\]

\[
\langle i_{\text{in}}(t) \rangle = \frac{v_{\text{in}}(t)}{2L}t_{\text{on}}(t)
\]

\[
\langle i_{\text{in}}(t) \rangle = \frac{v_{\text{in}}(t)}{R_{\text{in}}} = \frac{v_{\text{in}}(t)}{P_{\text{in}}}V_{\text{ac}}
\]

- On-time is constant
- Frequency is variable

\[
t_{\text{on}} = 18 \mu s
\]

\[
i_{\text{in}}(t) = \frac{V_{\text{ac}}\sqrt{2}t_{\text{on}}}{2L} \sin(\omega t)
\]

\[
i_L(t)
\]
Modulating the On-Time

- A capacitor is charged by a constant-current source.
- The error voltage modulates the toggling threshold and adjusts $t_{on}$.

- A maximum on-time clamp limits the power.
- This clamp can be adjusted based on the line level.
- Modulation around the 0-V input improves distortion.

$Q$ decreases
$Q$ increases
$P_{out}$ decreases
$P_{out}$ increases
Voltage-Mode Operation

- Constant on-time can be implemented in voltage-mode control
- No need to sense the input voltage!
- The inductor *peak current* follows the rectified voltage for a sinusoidal envelope
  - A multiplier is needed to sense the input voltage: increased power consumption
A Multiplier in the Chip

- The inductor current is scaled by the rectified voltage and follows the envelope.
- A small offset is added to the multiplier and effectively reduces $F_{sw}$ near 0 V.

\[ k_{off} = 0.0417 \]
\[ k_{mult} = 0.65 \]

Offset limits $F_{sw}$ excursion
Harmonic Distortion Enhancer

- The front-end capacitor holds some residual voltage near zero crossing
- A THD enhancer typically forces a higher on-time at low input voltage

Front-end capacitor does not discharge to 0 V
Average Mode Current

- The inductor current is shaped by a dedicated high-bandwidth loop

✓ Error between the inductor current and setpoint is minimized for best distortion

\[ k \cdot |v_{in}(t)| \]

\[ k \cdot |v_{in}(t)| \cdot V_{err} \]

\[ V_{in} = 100 \text{ V rms} \]

\[ P_{out} = 1 \text{ kW} \]

\[ i_{in}(t) \]

THD = 2.3% \( V_{in} = 100 \text{ V rms} \)

THD = 2.9% \( V_{in} = 230 \text{ V rms} \)
A High-Speed Current Loop

- It is important to ensure the fast and precise tracking of the current envelope
- The current loop must exhibit a wide bandwidth, e.g. 10 kHz typically

From control circuitry
Predictive Power Factor

- Most of the PFC circuits do sense the input voltage to build the control law
- Predictive timing generates PWM control without high-voltage sensing

The input current is the inductor current

\[ i_{in}(t) = i_L(t) \]

\[ \langle i_{in}(t) \rangle = \langle i_L(t) \rangle \]

Set the control law to program \( D_{off}(t) \)

\[ D_{off}(t) = \frac{R_e}{V_{out}} \left| \frac{v_{in}(t)}{R_e} \right| \]

Average values

Instantaneous variables

No Input Voltage Sensing

- By modulating the off-time duration across the input line, resistive input is ensured
- The input current is sensed via a shunt and averaged through a low-pass filter
- The error voltage adjusts the capacitor charging current and hence off-time duration

\[ I_{ch} = g_m V_e \]

\[ v_+ (t) = \frac{I_{ch}}{C_{ch}} t = \frac{g_m V_e}{C_{ch}} t \]

\[ v_- (t) = \langle i_L (t) \rangle R_s \]

\[ v_+ = v_- \quad \text{toggling} \]

\[ g_m V_e \frac{T_{off}}{C_{ch}} = \langle i_L (t) \rangle R_s \]

\[ D_{off} (t) = \frac{\langle i_L (t) \rangle R_s}{V_e g_m T_{sw}} \]

Simulation Example

- The application circuit is simple and requires a specific off-time modulator.
- A dedicated amplifier shapes the negative input current via a shunt.

The average off-time is modulated along the input sinewave.
Simulation Results

- The input current waveform is perfectly sinusoidal and undistorted

\[ i_{in}(t) \]

\[ i_{L}(t) \]

\( V_{in} = 100 \text{ V rms, } P_{out} = 1 \text{ kW} \)

Distortion data:

\( P_{out} = 1 \text{ kW} \)

\( V_{in} = 100 \text{ V rms THD} = 3\% \)

\( V_{in} = 230 \text{ V rms THD} = 6\% \)

Regulated output voltage
Single-Stage Converter

- It is possible to combine a PFC function with a flyback converter
- Very popular in lighting applications where bandwidth is naturally low

- Operates in quasi-resonant mode
- Power factor is usually greater than 0.9
- Constant on-time voltage-mode operation

Typical operating waveforms – 120 V rms
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A PFC is usually a boost converter operated in different conduction modes:

- Continuous Conduction Mode or CCM: high-power system, usually > 300 W
- Boundary/Borderline Conduction Mode or BCM: small to moderate power < 300 W
- Many derived structures like interleaved or totem-pole for higher power levels

The PFC controller implements a control law: how to force a sinusoidal input current?

- In BCM converters, it is usually a constant on-time control, voltage- or current-mode
- In CCM, there are usually proprietary control laws optimizing distortion and efficiency

Regardless of the implementation, loop analysis is important to guarantee a stable and reliable operation
Modeling a Power Factor Correction Stage

- Several ways exist to model switching converters
  - State-space averaging (SSA), PWM switch model, 1\textsuperscript{st}-order approximation etc.
  - A PFC is a slow system in essence with crossover frequency below 10 Hz
  - 1\textsuperscript{st}-order approximation averages power without considering switching mechanism

- If the load is a regulated switching converter, the incremental resistance is negative
A General Formula to Express the Output Power

- A generic PFC control law obeys the following formula:

\[
P_{in,avg} = \frac{K \cdot V_{in,rms}^m \cdot V_{control}^n}{V_{out}}
\]

- \(m\) characterizes the input-voltage feed-forward
- \(n\) is 1 in general for predictive-sensing stages
- \(K\) is a constant which depends on the modulator, \(L, R_{sense}\) etc.

- This is a large-signal expression which needs to be linearized
- The corresponding model does not predict high-frequency phenomenon like RHPZ
- Perfect for low-frequency approach of a naturally-slow PFC stage
- Works for any type of operation, CCM, CrM/BCM, fixed or variable frequency etc.

\(i_L(t)\)  
CCM, fixed frequency

\(i_L(t)\)  
CrM, variable frequency

Example with CrM Power Factor Correction

- The power transmitted by a power stage operated in CrM obeys the formula:

\[
P_{\text{in,avg}} = \frac{V_{\text{ac}}^2}{2L} G_{\text{PWM}} V_{\text{err}}
\]

- \(G_{\text{PWM}}\) represents the modulator small-signal gain
- \(L\) is the boost inductor value

100% efficiency

\[
I_{\text{out}} = \frac{V_{\text{ac}}^2}{2LV_{\text{out}}} G_{\text{PWM}} V_{\text{err}}
\]

- \(P_{\text{in}} = P_{\text{out}}\)

- Run partial differentiation to obtain small-signal coefficients:

\[
\hat{i}_{\text{out}} = \frac{\partial}{\partial V_{\text{out}}} \left( \frac{V_{\text{ac}}^2}{2L} \frac{G_{\text{PWM}} V_{\text{err}}}{V_{\text{out}}} \right) \bigg|_{\hat{V}_{\text{err}} = 0} \hat{v}_{\text{out}} + \frac{\partial}{\partial V_{\text{err}}} \left( \frac{V_{\text{ac}}^2}{2L} \frac{G_{\text{PWM}} V_{\text{err}}}{V_{\text{out}}} \right) \bigg|_{\hat{v}_{\text{out}} = 0} \hat{v}_{\text{err}}
\]
Modeling a Power Factor Correction Stage

- From the small-signal equation, build the complete simplified model

\[
H(s) = H_0 \approx \frac{1}{1 + \frac{s}{\omega_p}} \approx \frac{1}{1 + \frac{s}{\omega_z}}
\]

\[
H_0 = \frac{V_{ac}^2}{4L} \frac{R_{load} G_{PWM}}{V_{out}}
\]

\[
\omega_p \approx \frac{2}{R_{load} C_{bulk}}
\]

- Assume the following specifications:

\[
\begin{align*}
P_{in} &= 144 \text{ W} \\
V_{out} &= 380 \text{ V} \\
L &= 250 \mu\text{H} \\
C_{bulk} &= 200 \mu\text{F} \\
R_{load} &= 1 \text{ k}\Omega
\end{align*}
\]

\[
H_0 = 78 \approx 38 \text{ dB}
\]

\[
f_p = 1.6 \text{ Hz}
\]

\[
V_{in} = 90 \text{ V rms}
\]

\[
\arg[H_{LL}(j2\pi f_k)] \approx \frac{180}{\pi}
\]

\[
20 \cdot \log |H_{LL}(j2\pi f_k)|
\]

Plot power stage (LL)
Compensation Strategy for the PFC

- Without specific treatment, dc gain changes with line input squared
- For ratio of 2.3 between 265 V and 90 V rms input, gain changes by $2.94^2 \approx 9$
  
  Select a crossover $f_c = 50$ Hz at a 265-V input to keep at least 8-10 Hz at lowest line

\[
|H(f_c)| = \frac{H_0}{\left(1 + \left(\frac{f_c}{f_p}\right)^2\right)^{\text{gain excess}}} = 26.6
\]

\[
\angle H(f_c) = -\tan^{-1}\left(\frac{f_c}{f_p}\right) = -88^\circ
\]

- Bring a 1/26.6 or 28.5-dB attenuation at 50 Hz
- For a 70° phase margin, boost the phase by:
  
  \[
  \text{boost} = 70^\circ - (-88) - 90 = 68^\circ
  \]

- One pole and one zero to boost the phase by 68°
  
  \[
  f_p = 260 \text{ Hz}
  \]
  
  \[
  f_z = 9.6 \text{ Hz}
  \]
Check Compensated Response

- A type 2 compensator is needed

- Check crossover and phase margin at the input line extremes \( T(s) = H(s)G(s) \)

\[
\begin{align*}
    V_{\text{out}}(s) \quad \text{HV output} \\
    g_m \quad \text{Operational Transconductance Amplifier (OTA)} \\
    V_{\text{ref}} \\
    C_1 \\
    C_2 \\
    R_{\text{lower}} \\
    V_{\text{err}}(s) \\
    \text{Check crossover and phase margin at the input line extremes}
\end{align*}
\]

\[
\begin{align*}
    V_{\text{out}}(s) \quad \text{HV output} \\
    R_1 \\
    R_2 \\
    C_1 \\
    C_2 \\
    V_{\text{ref}} \\
    \text{Operational Amplifier (op-amp)}
\end{align*}
\]

Low line, 90 V rms

High line, 265 V rms

\( f_c = 8.5 \, \text{Hz} \quad \phi_m = 50^\circ \)

\( f_c = 50 \, \text{Hz} \quad \phi_m = 70^\circ \)
Simulate the Converter after Compensation

- SIMPLIS® is well suited for simulating power factor correction stages
- The program can plot the ac response from a switching circuit and simulates fast

Templates can be freely downloaded from https://cbasso.pagesperso-orange.fr/Spice.htm
Check Transient Response is Acceptable

- The output current is stepped from 400 to 600 mA at the lowest 90-V rms input voltage.
Transient Response at High Line

- In high-line conditions, the PFC is stable but given the higher crossover, distortion suffers.

\[ V_{in} = 265 \text{ V rms} \]
Compensating a CCM PFC

- We take the example of a 1-kW PFC operated in continuous conduction mode
- An averaged model is used to extract the control-to-output transfer function
- The predictive controller is the NCP1654 from onsemi
Closing the Loop

- The control-to-output transfer function is obtained with an averaged SPICE model
- Some in-line behavioral equations describe the controller’s internals

✔ Works in ac and transient analyzes
The Power Stage Response

- The control-to-output transfer function is the starting point for compensation
- Infer a compensation strategy by reading information from magnitude and phase

- Crossover cannot be too high otherwise ripple may pollute the control voltage
- If too high then ripple will bring distortion and produce third harmonic
- Too low brings an unacceptable slow transient response
- Without feedforward the crossover may theoretically move with a factor of 9 in high- and low-line conditions
- NCP1654 feedforward limits the change in crossover frequency

Select $f_c$ in high-line conditions to obtain 5-10 Hz at low line

$$f_{c,HL} = 20 \text{ Hz}$$
Check Loop Gain

- The dc input voltage in an ac analysis is the rms voltage of the source.
- Enter 100 V dc and 230 V dc for respective low- and high-line simulations.

Computed values:

- $V_{\text{rms}} = 230$
- $V_{\text{out}} = 400$
- $P_{\text{out}} = 1.3k$
- $L = 54u$
- $R_{\text{BOL}} = 82.5k$
- $R_{\text{BOU}} = 6.6\text{Meg}$
- $ROCP = 3.8k$
- $V_{p} = 2.5$
- $R_{\text{sense}} = 30m$
- $I_{b} = 100u$
- $R_{\text{upper}} = 3.975\text{Meg}$
- $R_{\text{lower}} = 25k$
- $f_{c} = 20$
- $G_{fc} = 36.7$
- $Ps = -60$
- $Pm = 60$
- $Gm = 200u$
- $\text{boost} = 30$
- $G = 14.621771745m$
- $k = 1.73205080757$
- $f_{p} = 34.6410161514$
- $f_{z} = 11.5470053838$
- $a = 1.15470053838$
- $b = 1.15470053838$
- $R_{2} = 17.546126093k$
- $C_{1} = 785.54219388n$
- $C_{2} = 392.77109694n$

Compensator

$V_{\text{in}} = 230 \text{ V rms}$

$V_{\text{in}} = 100 \text{ V rms}$

$\angle G(f)$

$\angle T(f)$

$\angle T(f)$

$\angle G(f)$
Transient Response Performance

- The large-signal average model lends itself well to a transient simulation.
- The input current at low line shows a good harmonic distortion figure of 4.2%.

$\text{THD}_{LL} = 4.23\%$
$\text{THD}_{HL} = 6.33\%$

The output current is stepped from 300 W to 1.3 kW with a 1-A/µs slope.

The transient response is stable at low and high line.
Internal Digital Compensation

- The NCP1680 embeds an internal type 2 compensator
- A low-pass filter then follows to reduce the ripple contribution
- Mid-band gain is adjusted based on the input line value

\[ G(s) = \frac{V_{\text{err}}(s)}{V_{\text{out}}(s)} = -G_0 \frac{1 + \frac{\omega_z}{s}}{1 + \frac{s}{\omega_p}} \]

\[ G_0 \approx 13.6 \text{ dB} \]
\[ \omega_z \approx 1.44 \text{ Hz} \]
\[ \omega_p \approx 68 \text{ Hz} \]
A Low-Pass Filter Reduces Feedback Ripple

- A low-pass filter is inserted in series with the compensator
- The digital implementation of this filter brings efficient output ripple rejection
- The sampling frequency is adjusted depending on the line frequency

\[ y[n] = 0.5(u[n] + u[n-1]) \]

\[ G(s) \approx \frac{1 + \frac{s}{\omega Q_N} + \left(\frac{s}{\omega}\right)^2}{1 + \frac{s}{\omega Q_D} + \left(\frac{s}{\omega}\right)^2} \]

- Sampling frequency is \(4F_{\text{line}}\)
- It sets a notch at twice the line frequency
The digital filter is simulated with delay lines and fed by a Laplace expression.

Transfer function of the power stage

Resistive divider gain

Moving average low-pass filter

Type 2 compensator

Compensated loop gain
Typical Results for a 300-W Board

- The 300-W TPPFC features a constant crossover frequency regardless of input line

\[ |T(f)| \]

High line
Low line

Crossover frequency is almost unchanged

\[ V_{in} = 100 \text{ V rms} \]

\[ V_{in} = 230 \text{ V rms} \]
Agenda

- Notions of Power Factor
- Power Factor Correction Structures
- Processing the Power
- Loop Compensation of a PFC
- Solutions from Future Suppliers
Power Factor Controller Selection

- The selection of a PFC controller depends on various parameters:
  - Constant on-time in BCM for low power, up to 200-300 W
  - Want higher power in BCM: go for interleaved PFC
  - Average mode control and CCM for high power, up to several kW
  - Need for optimized efficiency? Go for multi-mode operation
  - Need for the best efficiency? Go for a totem-pole PFC
  - For compact design, go for a combo chip combining a PFC and a switching controller

- TEA2017: PFC and LLC
- FAN6921BMR: PFC and QR flyback
- IDP2308: PFC and LLC
- STCMB1: PFC and LLC
- HR1213: PFC and LLC
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## PFC Controllers from Onsemi

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PFC Controllers from NXP

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✓ The two standalone PFCs can be teamed up with LLC controller TEA19161T

# PFC Controllers from Infineon

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✓ ICE3PCS03G and ICE3PCS01G include an internal digital compensation

## PFC Controllers from STMicroelectronics

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Conclusion

- Nonlinear loads force the unnecessary circulation of reactive power
- Reactive power flows in the grid and heats up distribution wires
- Mains rectification brings a poor power factor and distorts the current
  - Power factor correction forces the absorption of a sinusoidal current
  - It reduces the circulating reactive power and reduces the rms current
- The boost converter is a popular structure and can operate in:
  - Borderline conduction mode up to 200-300 W
  - Continuous conduction mode for high output levels beyond 1 kW
  - Multi-mode combine best of both worlds for optimized efficiency
- The totem-pole PFC becomes popular owing to wide-bandgap components
- A PFC is a closed-loop system: pay attention to the stability