FUTURE ELECTRONICS

A WT Microelectronics Company

Trade Secrets of the Flyback Converter

Theory and Simulation

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Agenda

- Theory of operation
- Controlling the Converter
- Current-Mode Instabilities
- The Right-Half-Plane Zero
- Closing the Loop with the Flyback Converter

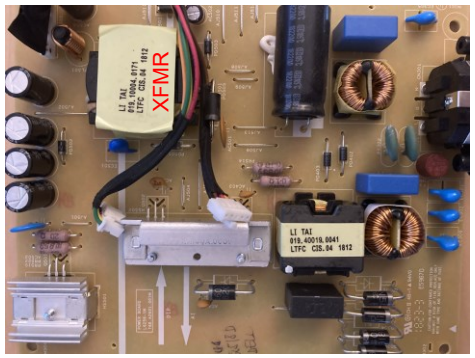
The Flyback Converter is Everywhere

- You can find a flyback converter in numerous consumer products:

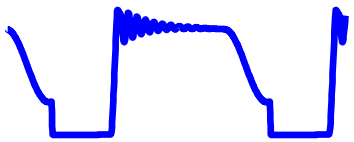
✓ Ac-dc chargers, for notebooks (90 W), cell-phone chargers (10 W or so), TVs etc.

✓ It can be a single or multi-output type, like in a set-top box or monitor (20-50 W)

DELL U2518D
12-V power
supply board



Controlled by combo chip
LD7790, PFC + QR
converter



✓ The converter can be operated with one or two switches, with or without sync rect

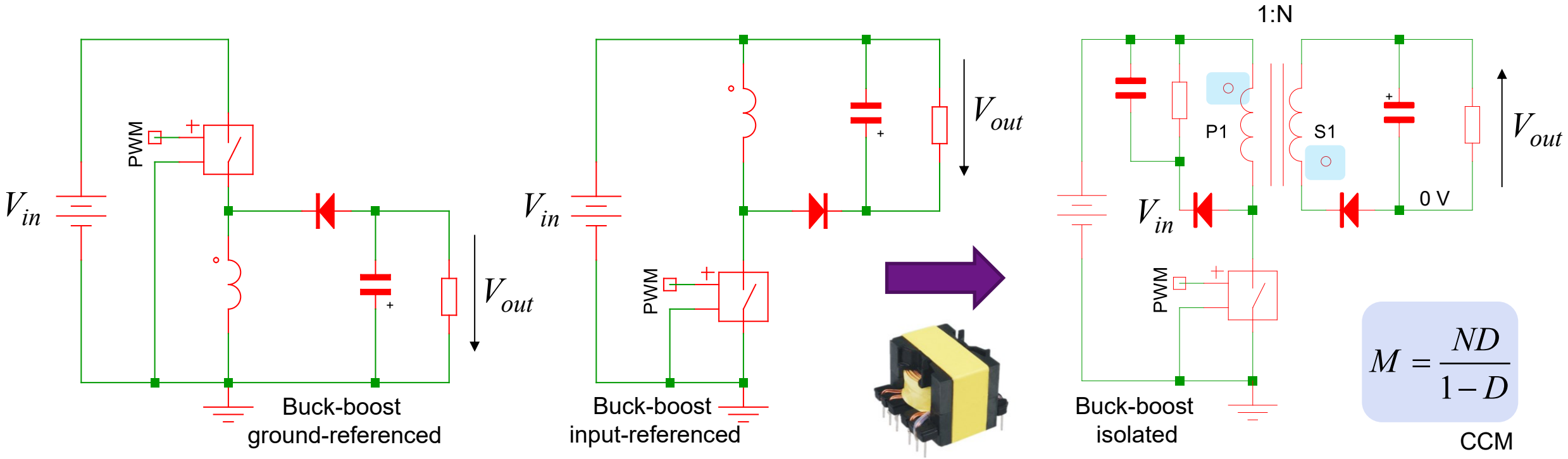
✓ It can be used at a fixed or variable switching frequency

✓ Feedback can be implemented with an optocoupler or an auxiliary winding

✓ High-switching-frequency versions implement active-clamp or asymmetrical half-bridge

A Transformer for Galvanic Isolation

- The flyback converter derives from the buck-boost topology
- The converter can deliver positive or negative levels, increase or decrease V_{in}



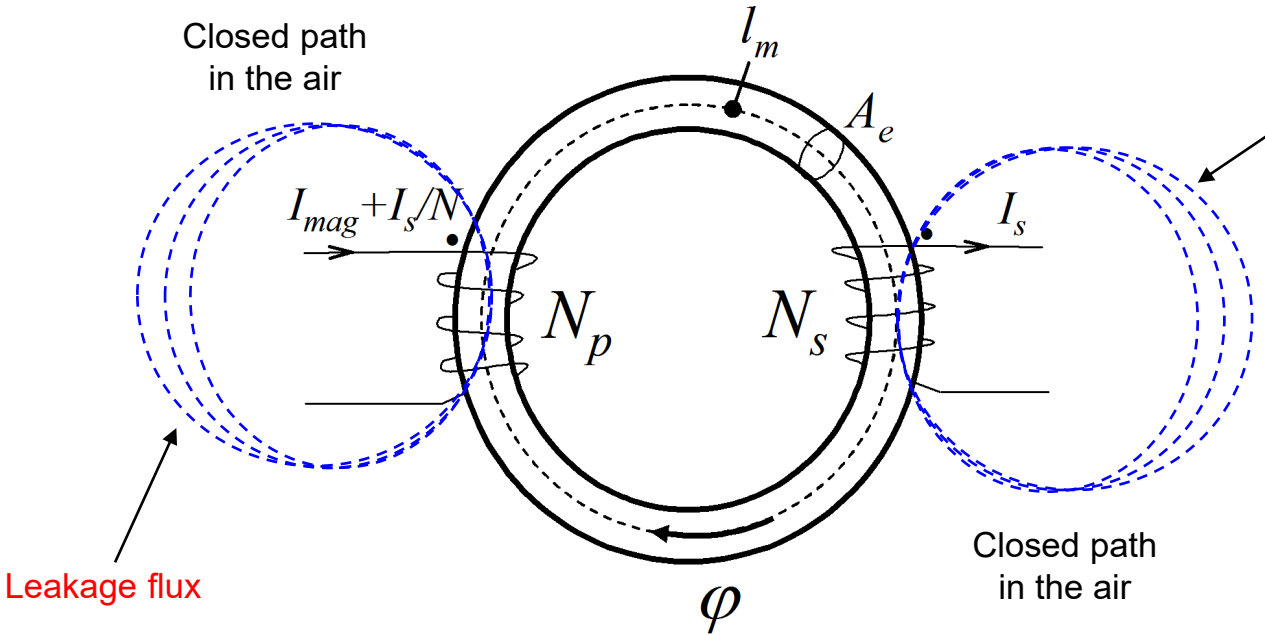
- The flyback converter can be identified with its winding dots located in opposite ends

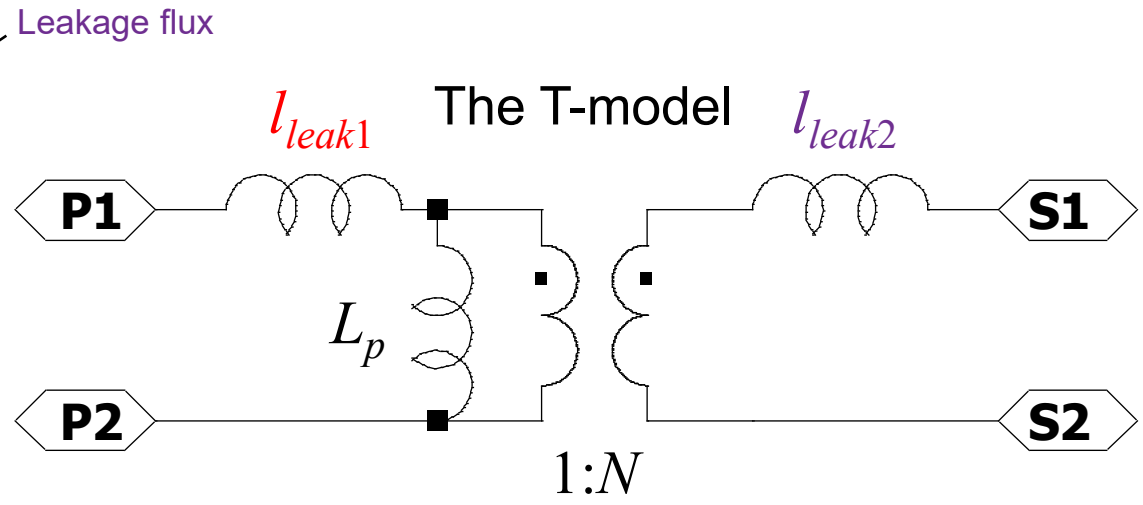
✓ A clamping network is necessary to protect the power switch

C. Basso, *The Dark Side of the Flyback Converter*, APEC Professional Seminar 2011, Fort Worth (TX) 2011

The Perfidious Leakage Inductance

- The coupling between the transformer windings is not perfect
- Some induction lines close in the air and create a leakage flux



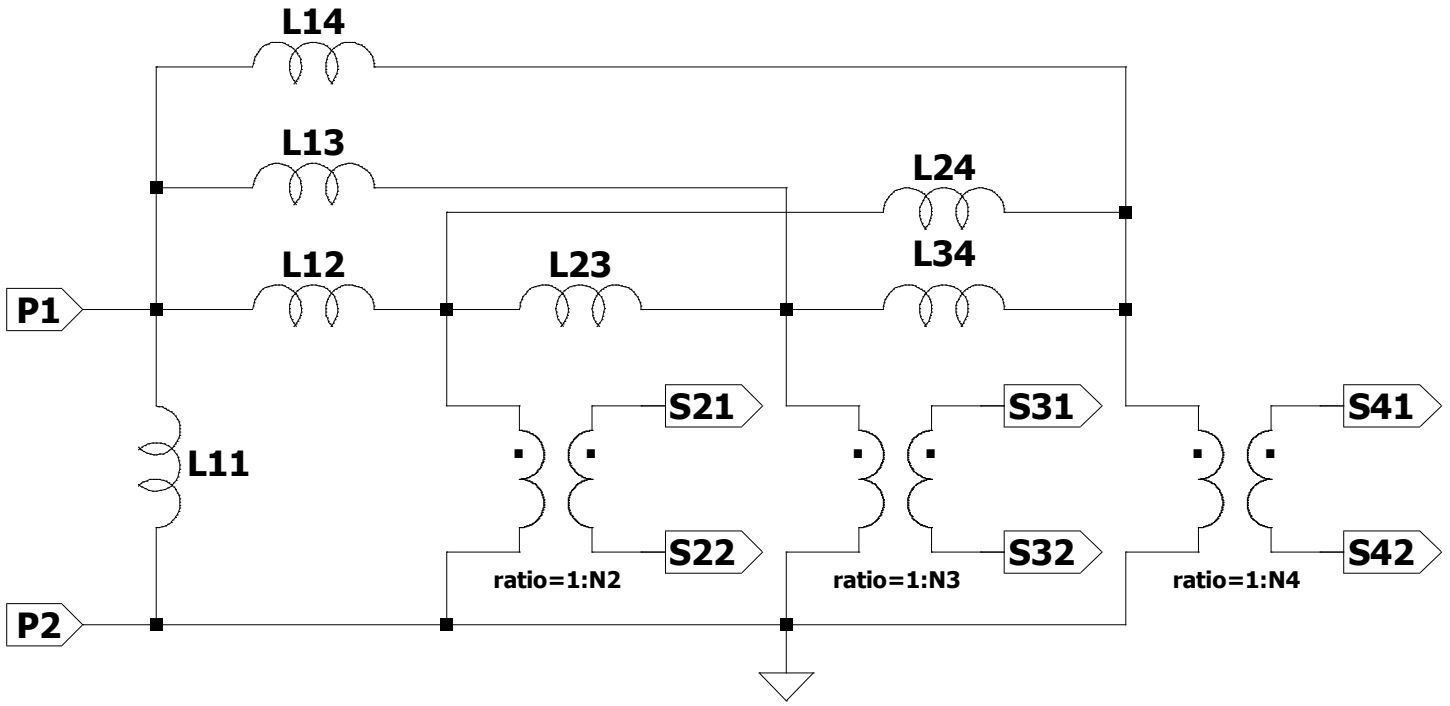


- This phenomenon can be modeled by so-called *leakage* inductances
- These inductances do not depend on the core but on windings geometry

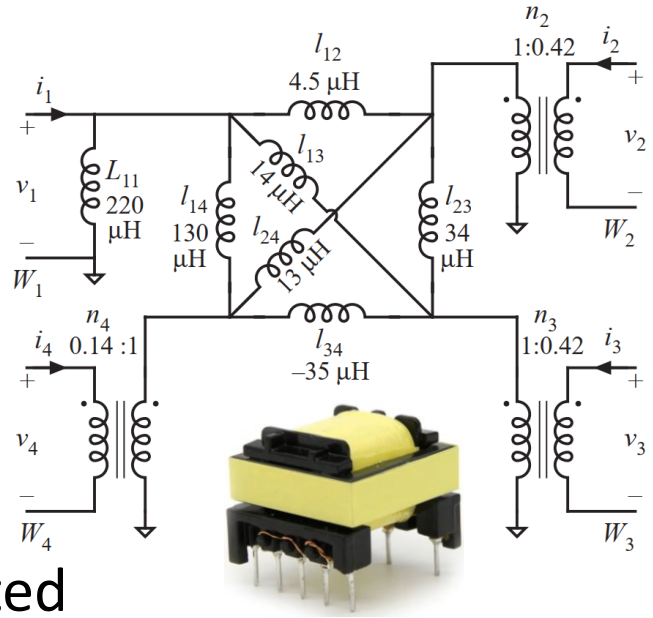
S. Hsu, R.D. Middlebrook, S. Ćuk, *Transformer Modelling and Design for Leakage Control*, Advances in Switched-Mode Power Conversion, vols. 1 and 2, TESLAco, 1983

The Extended Cantilever Model

- The T-model is well suited for a simple 2-winding configuration
- It cannot explain and predict cross-regulation mechanisms in multi-output applications
- ✓ The extended cantilever model is well suited for this purpose



Typical parameters extraction for a 4-winding transformer



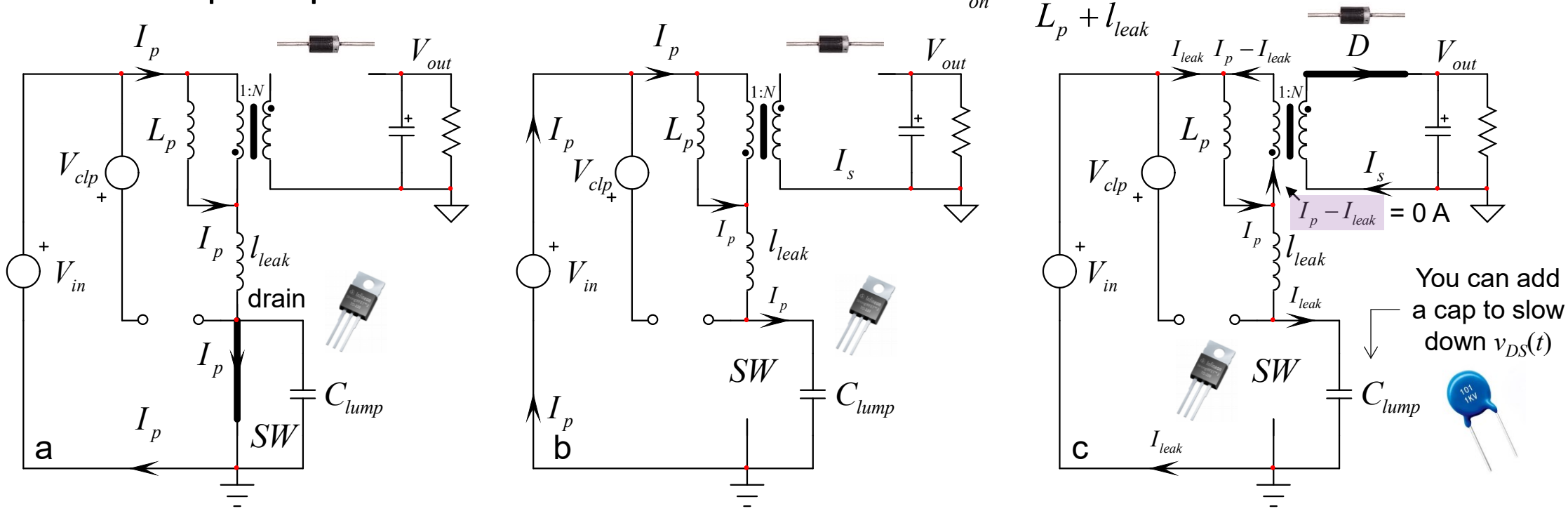
- Parameters extraction for this model is painful and complicated

❖ I have rarely seen it implemented in industrial projects

R. W. Erickson and D. Maksimović, *A multiple-winding magnetics model having directly measurable parameters*, *PESC 98. 29th Annual IEEE Power Electronics Specialists Conference*

Theory of Operation – I

- The switch turns on and magnetizes the series inductances L_p and l_{leak}
- The on-slope depends on both inductance values: $S_{on} = \dfrac{V_{in}}{L_p + l_{leak}}$



- At turn-off, the primary current diverts in the capacitance lumped at the drain

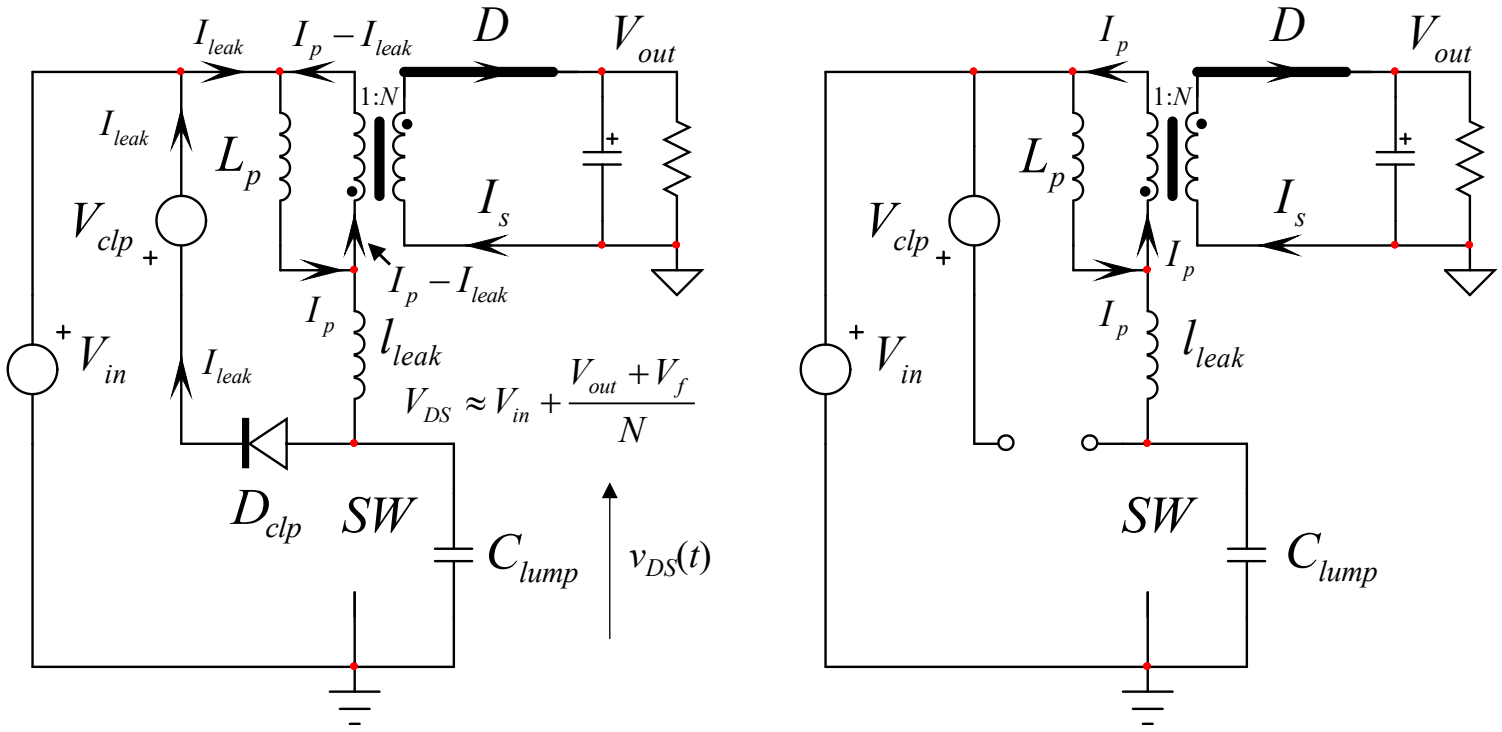
✓ The drain voltage quickly rises with a slope depending on I_p and C_{lump}: $S_{drain} \approx \dfrac{I_{peak}}{C_{lump}}$

✓ The secondary diode is biased but no current circulates in the secondary yet

Theory of Operation – II

- D_{clp} conducts and the leakage inductance reset period begins: $S_{off,l_{leak}} = -\dfrac{V_{clp} - \dfrac{V_{out}+V_f}{N}}{l_{leak}}$

✓ Current begins to flow in the secondary diode D and starts from zero



- The secondary current I_s rises as l_{leak} depletes

✓ It is maximal when the leakage inductance is reset

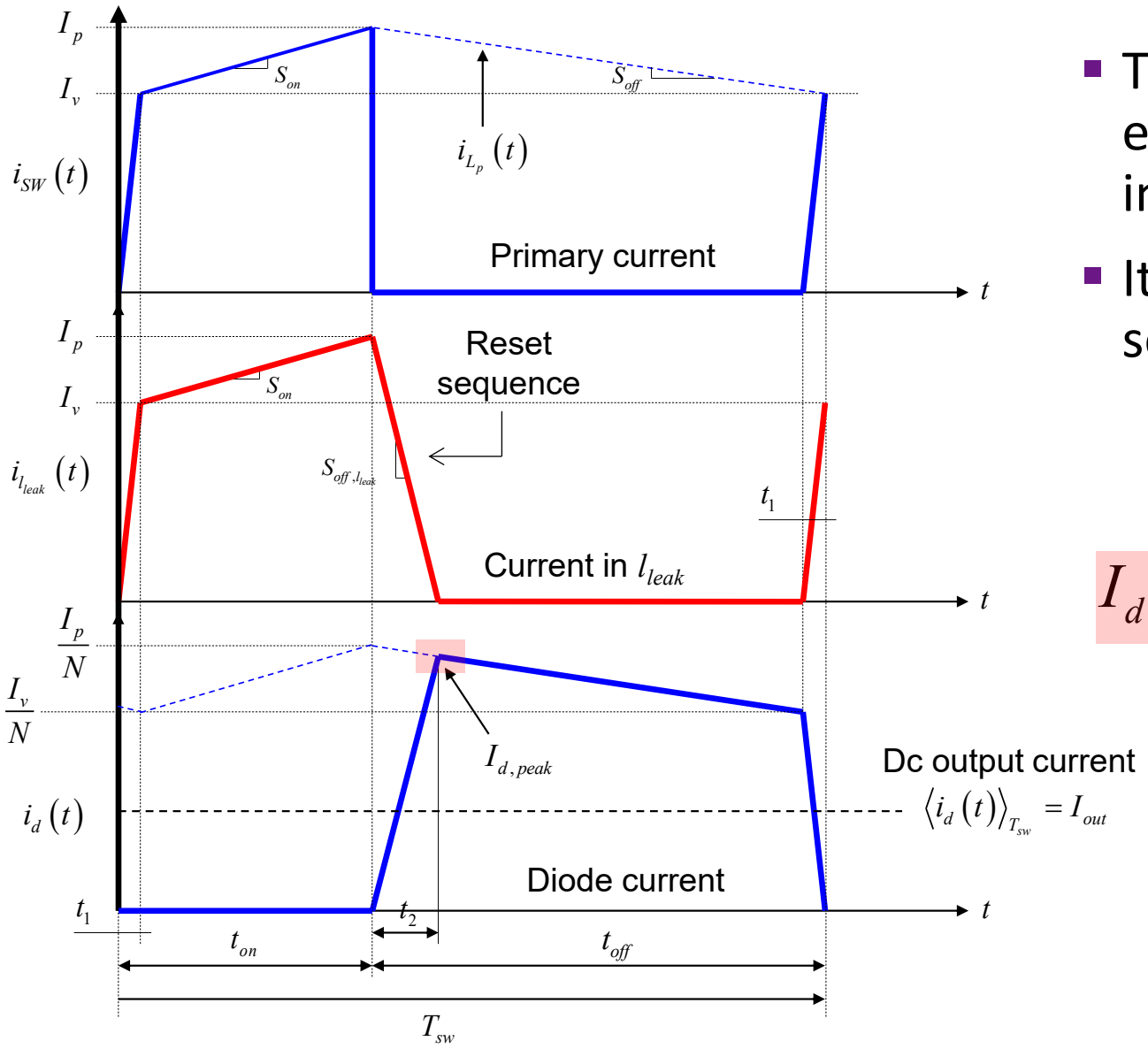
❖ This current is unfortunately not I_p/N

The current in the clamping network is not exactly the current at the switching opening. This is because C_{lump} has diverted some energy to charge up and depleted a bit L_p and l_{leak}

$$I_{leak} = \sqrt{I_p^{\,2} - \frac{C_{lump}}{l_{leak}+L_p}\left(V_{in}+V_{clp}\right)^2}$$

Less losses in the clamping network!

Less Secondary Current than Expected



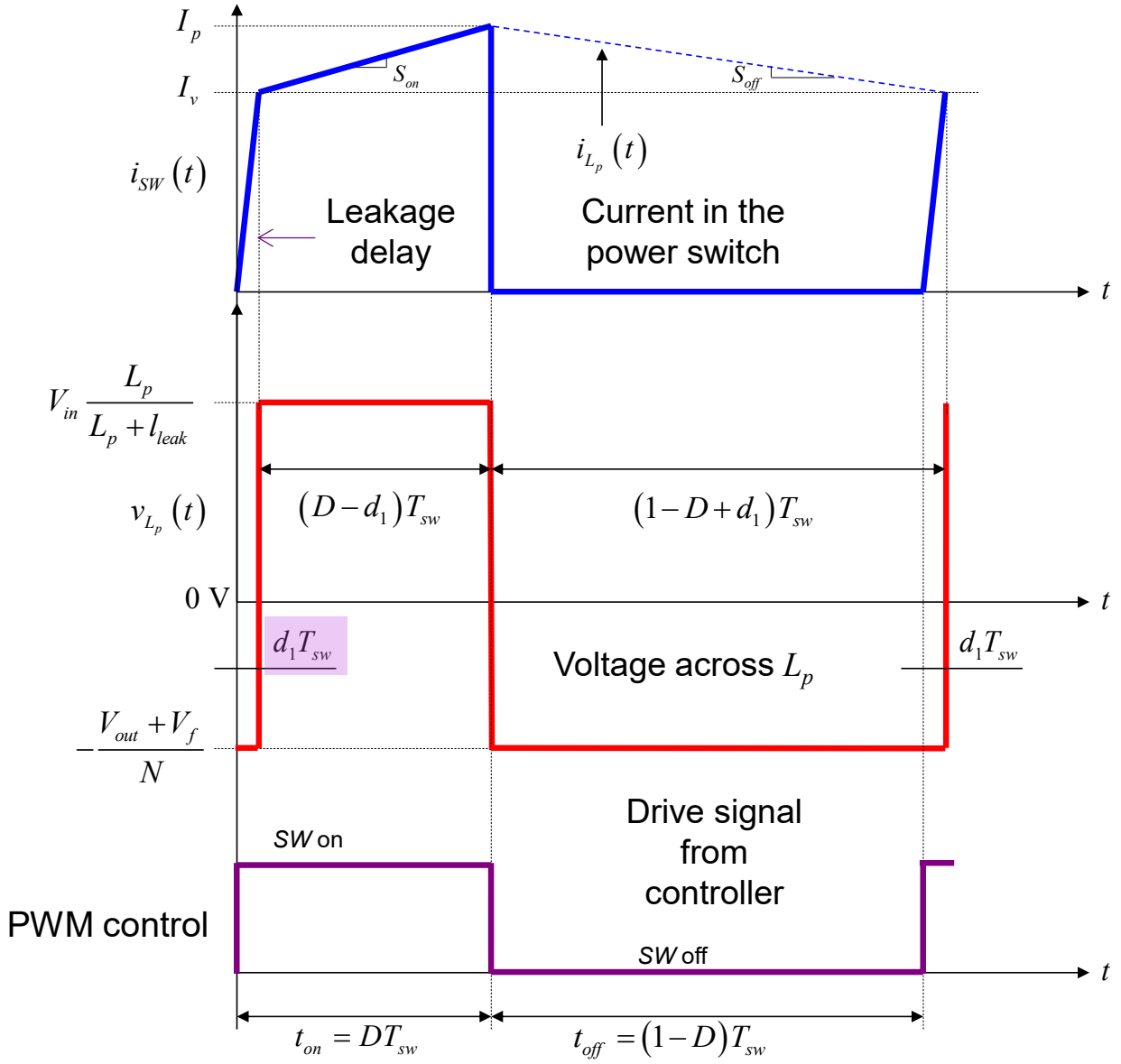
- The leakage inductance dissipates some energy stored in the magnetizing inductance
- It also delays the occurrence of the peak secondary current

$$I_{d,peak} = \frac{I_{peak}}{N}\left(1 - \frac{l_{leak}}{L_p}\frac{1}{\frac{NV_{clp}}{V_{out}+V_f} - 1}\right)$$

Theoretical value

Leakage inductance effects

Effective Duty Ratio



- When the switch turns on in CCM, the current does not jump to the valley current I_v
- The leakage inductance sets the current slope and affects the *real* duty ratio:

$$d_1=\frac{I_v l_{leak}}{\left(V_{in}+\dfrac{V_{out}}{N}\right)T_{sw}}$$

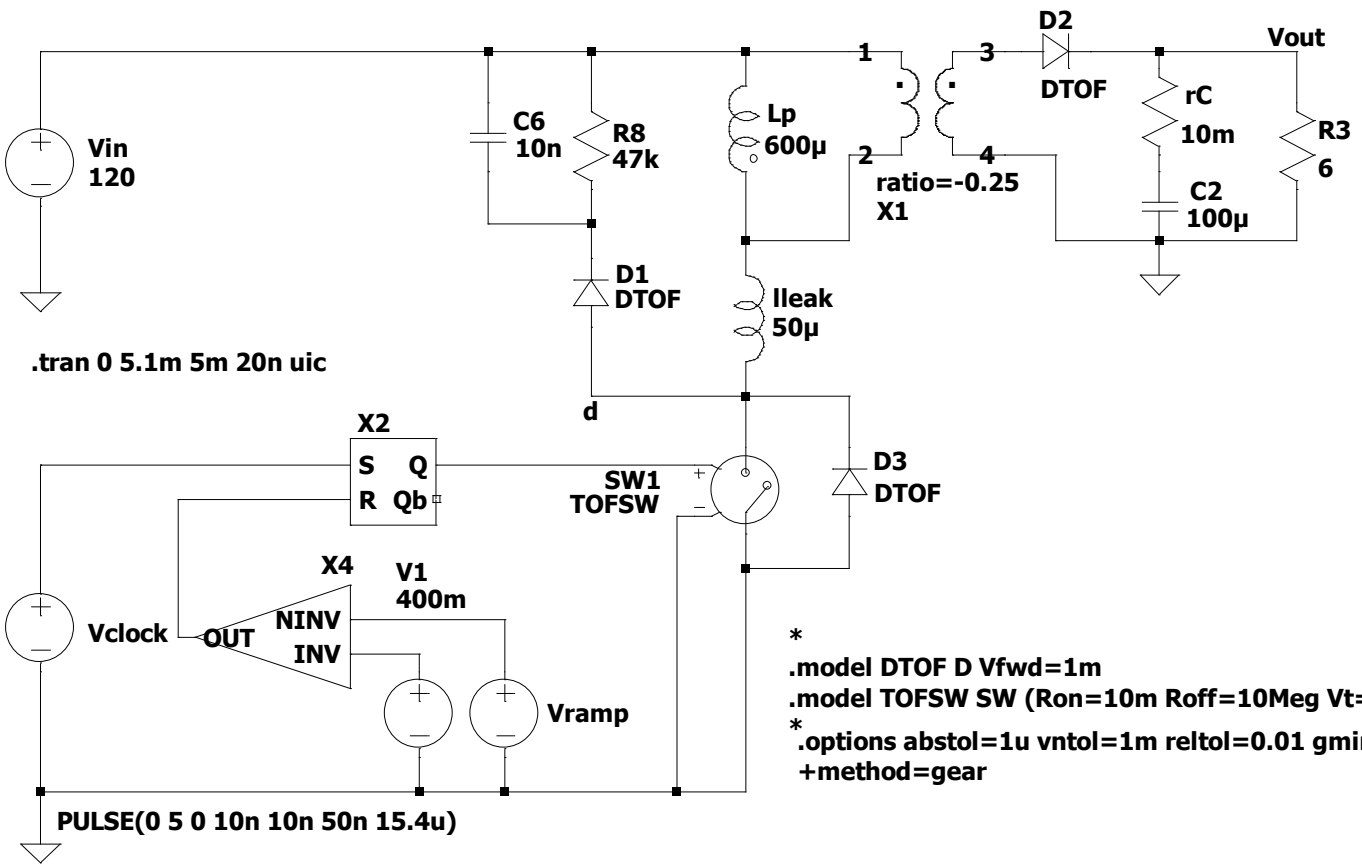
It is subtracted from the duty ratio D

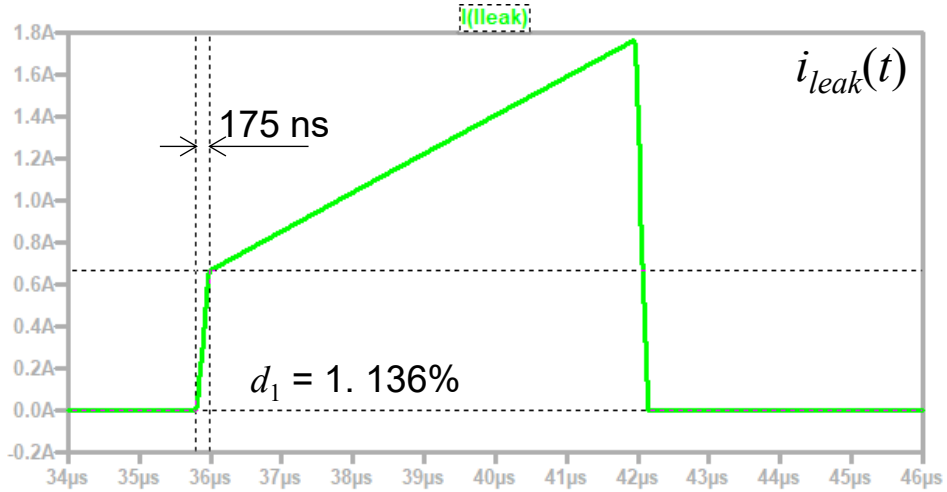
Effective duty ratio

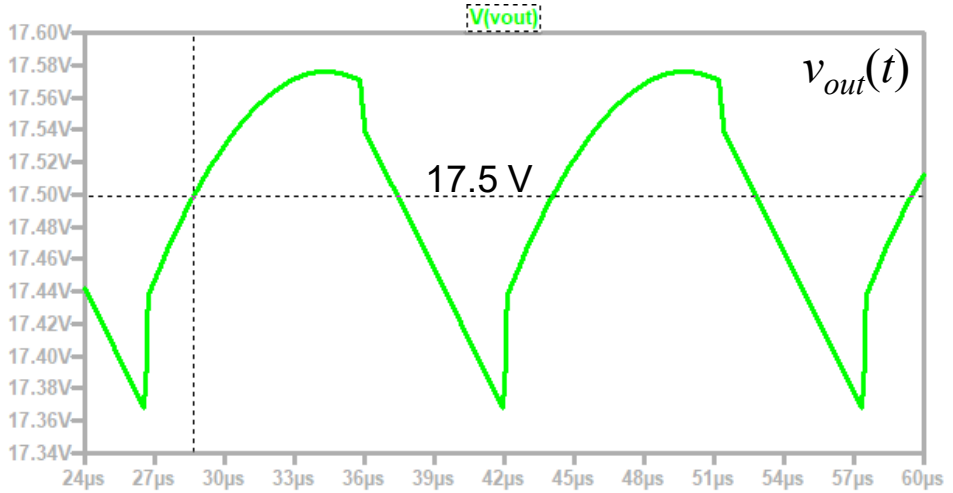
$$\frac{V_{out}}{V_{in}}=\frac{D-d_1}{1-D+d_1}N\frac{L_p}{L_p+l_{leak}}$$

Simulating Leakage Inductance Effects

- Simulations confirm a 193-ns delay at turn-on with 50 µH of leakage inductance

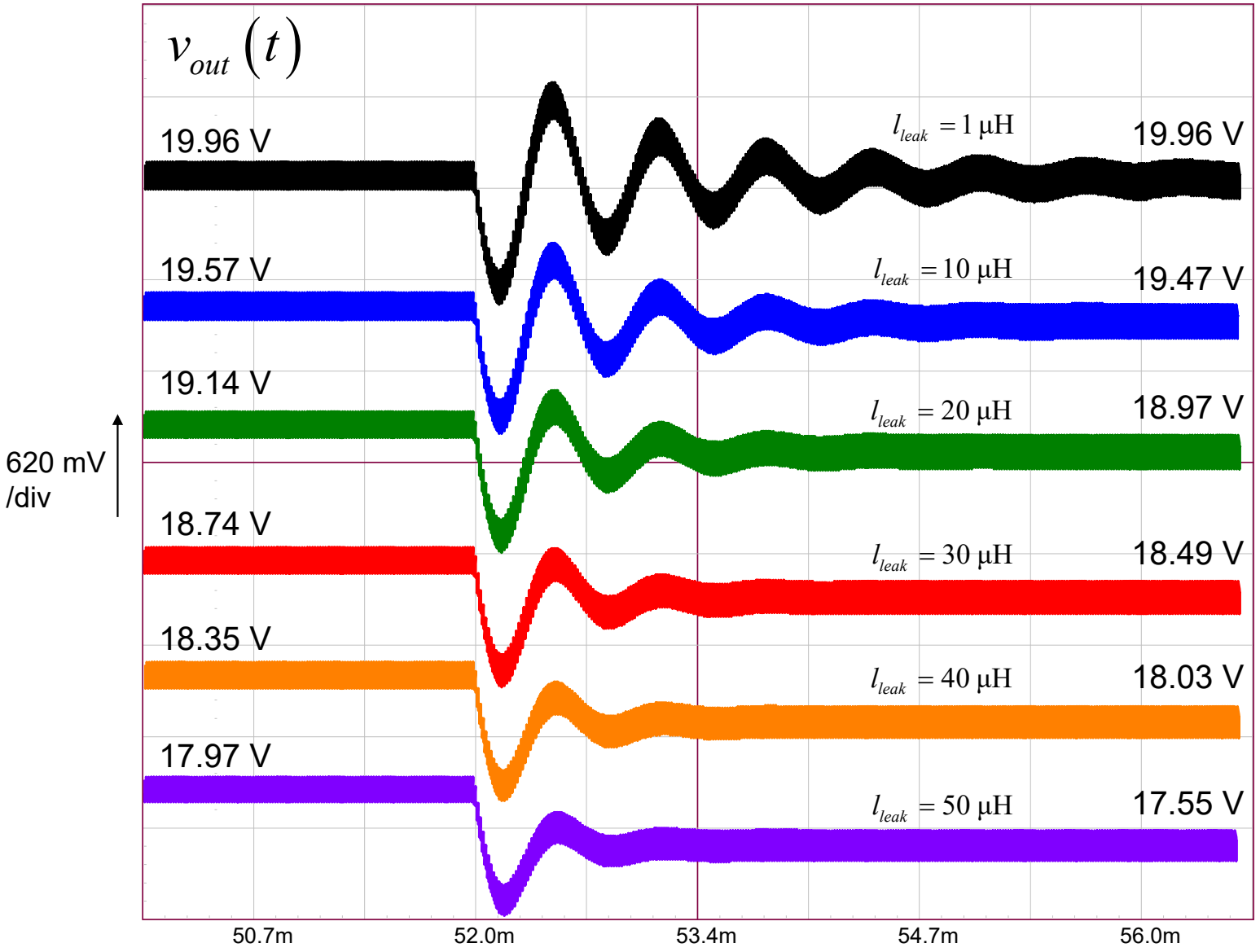






$$V_{out} = \frac{0.4 - 0.0175}{1 - 0.4 + 0.0175} \times 0.25 \times 120 \times \frac{600u}{600u + 50u} \approx 17.2 \text{ V}$$

Leakage Impact on Output Impedance



- A CCM flyback converter operated in voltage-mode control is a second-order system

✓ The leakage inductance contribution to efficiency damps the small-signal response

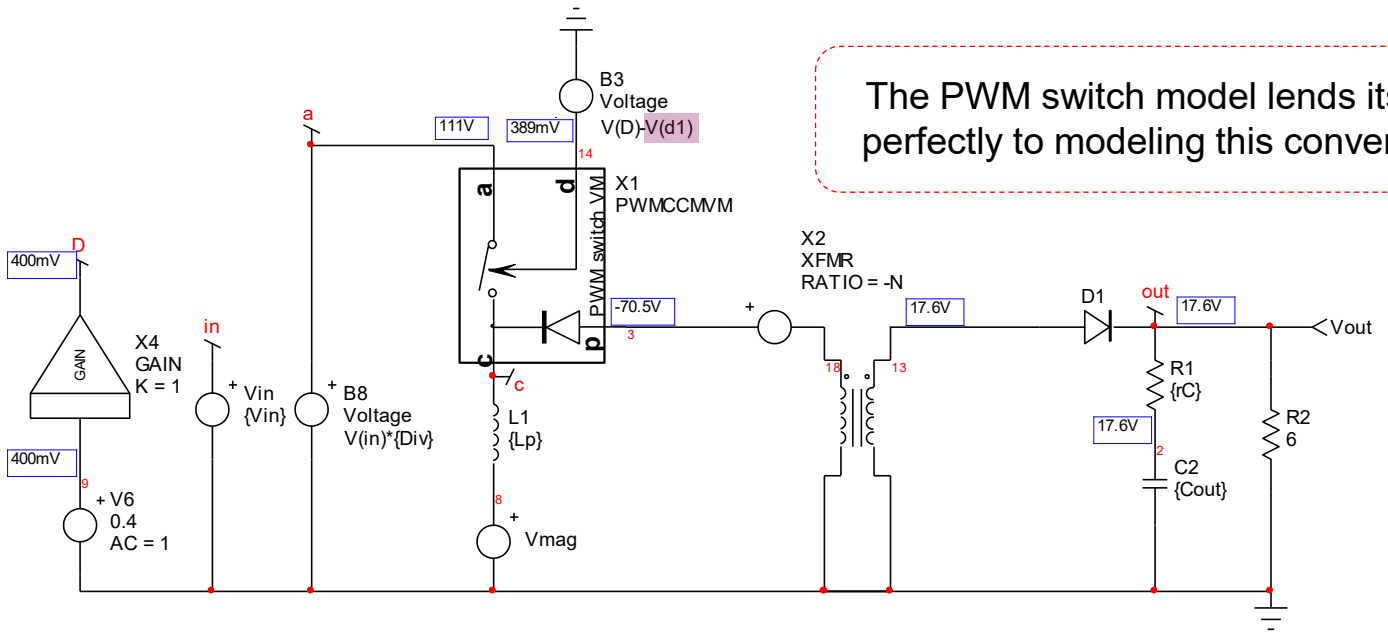
✓ The output impedance is also affected as l_{leak} increases

A Large-Signal Nonlinear Model

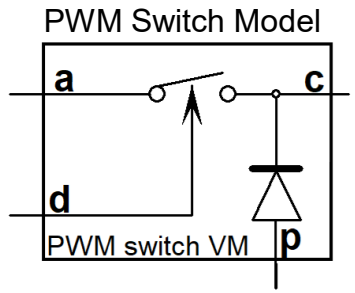
- The model needs validation before running the small-signal analysis

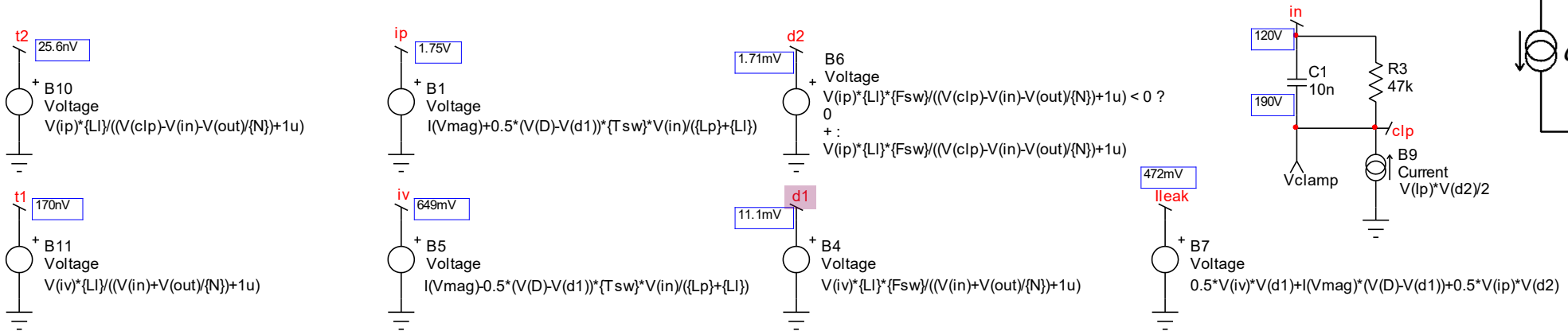
parameters

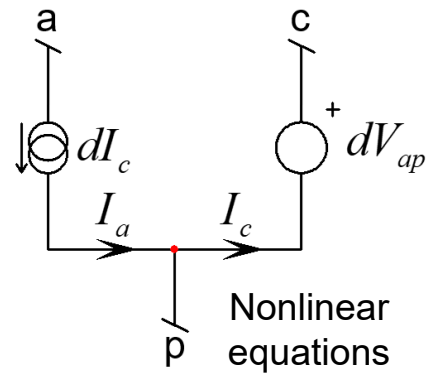
Vin=120
N=0.25
pi=3.14159
Lp=600u
Ll=50u
Fsw=65k
Tsw=1/Fsw
rC=10m
Cout=100u
Div=Lp/(Lp+Ll)



The PWM switch model lends itself perfectly to modeling this converter.



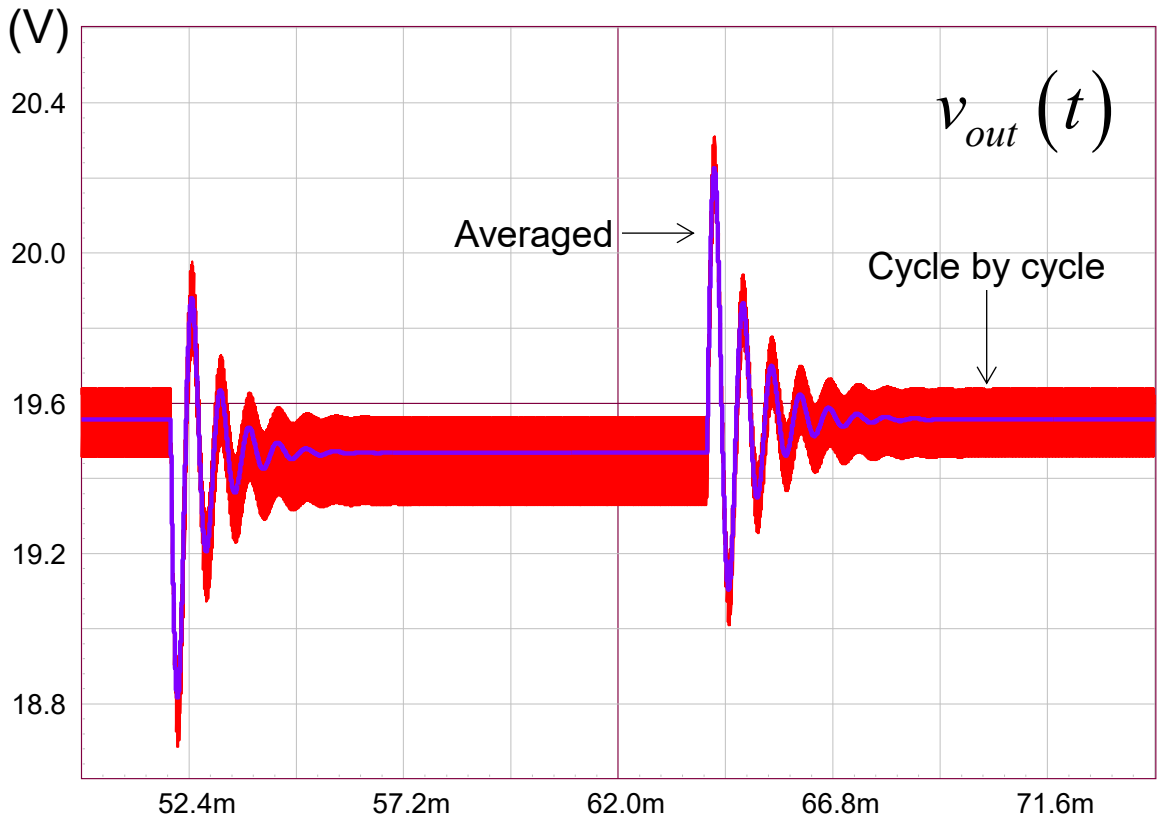


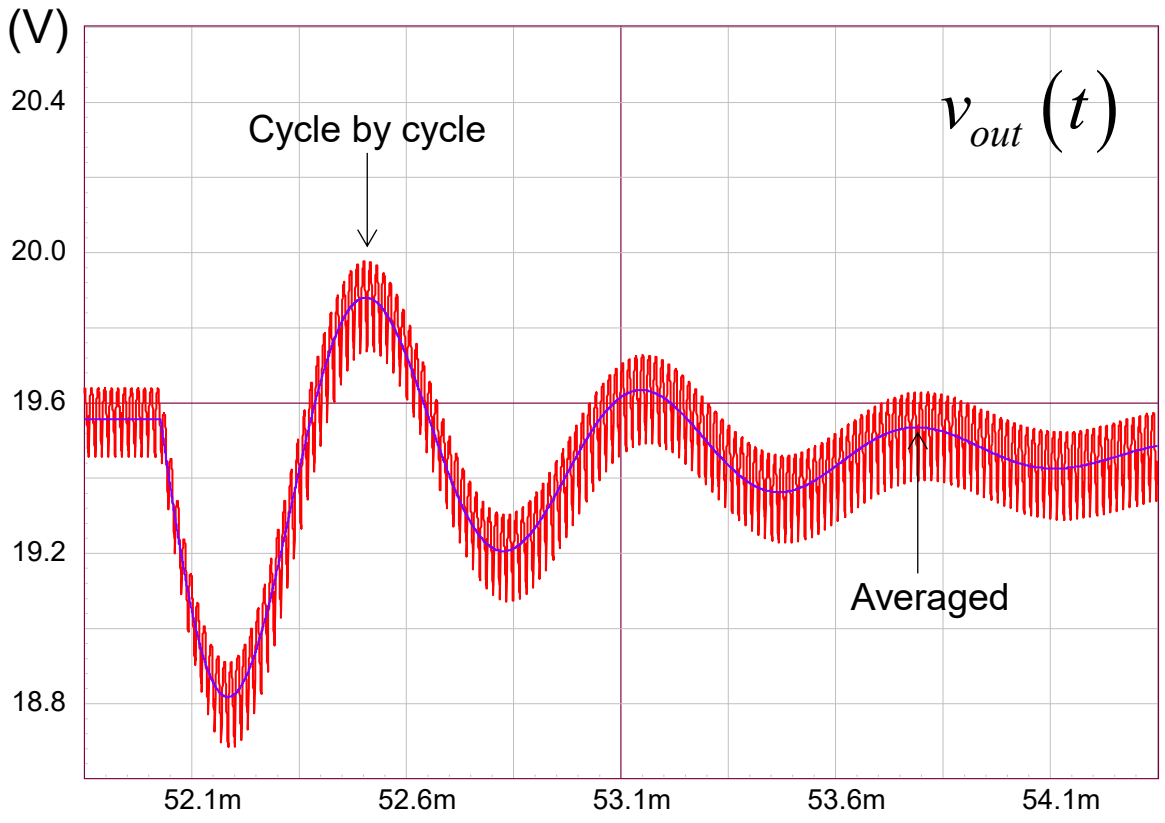


V. Vorpérian, *Simplified analysis of PWM converters using model of PWM switch. Continuous conduction mode*, in *IEEE Transactions on Aerospace and Electronic Systems*, May 1990

Validating the Model with a Load Step

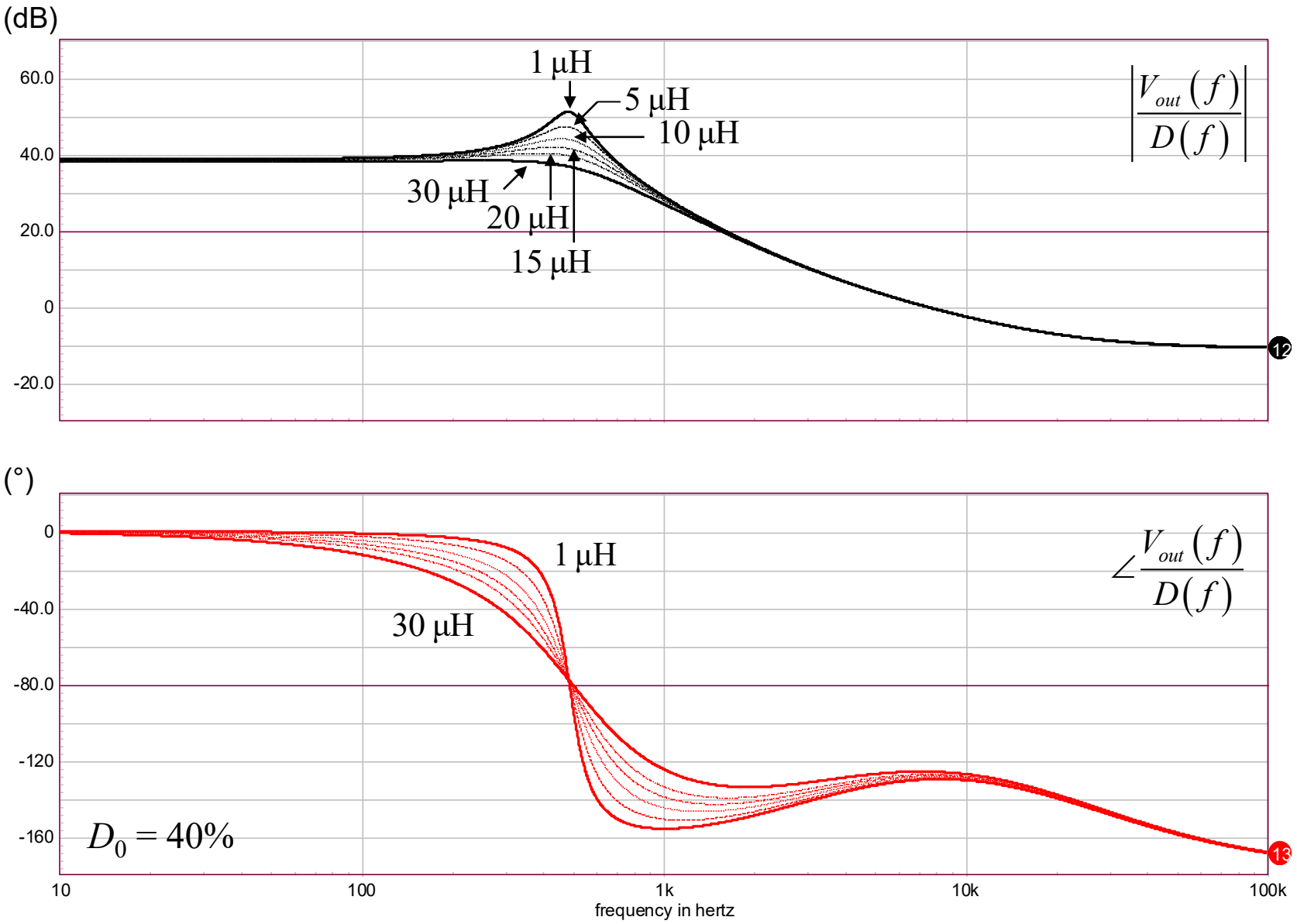
- It is important to check the dynamic responses and compare both
  - ✓ Transient waveforms must perfectly superimpose for validation



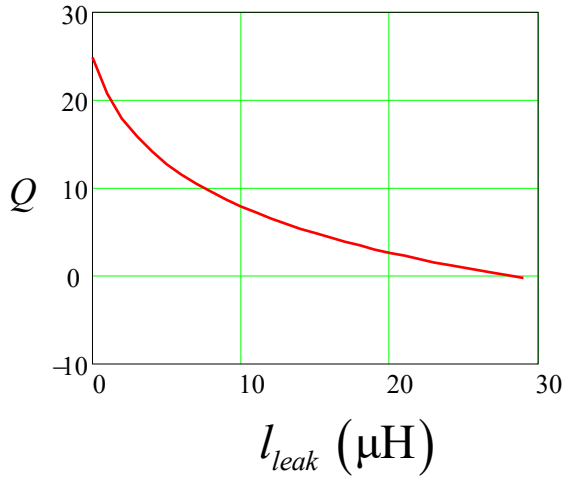


$$l_{leak} = 10\ \mu\text{H}$$

Control-to-Output Transfer Function

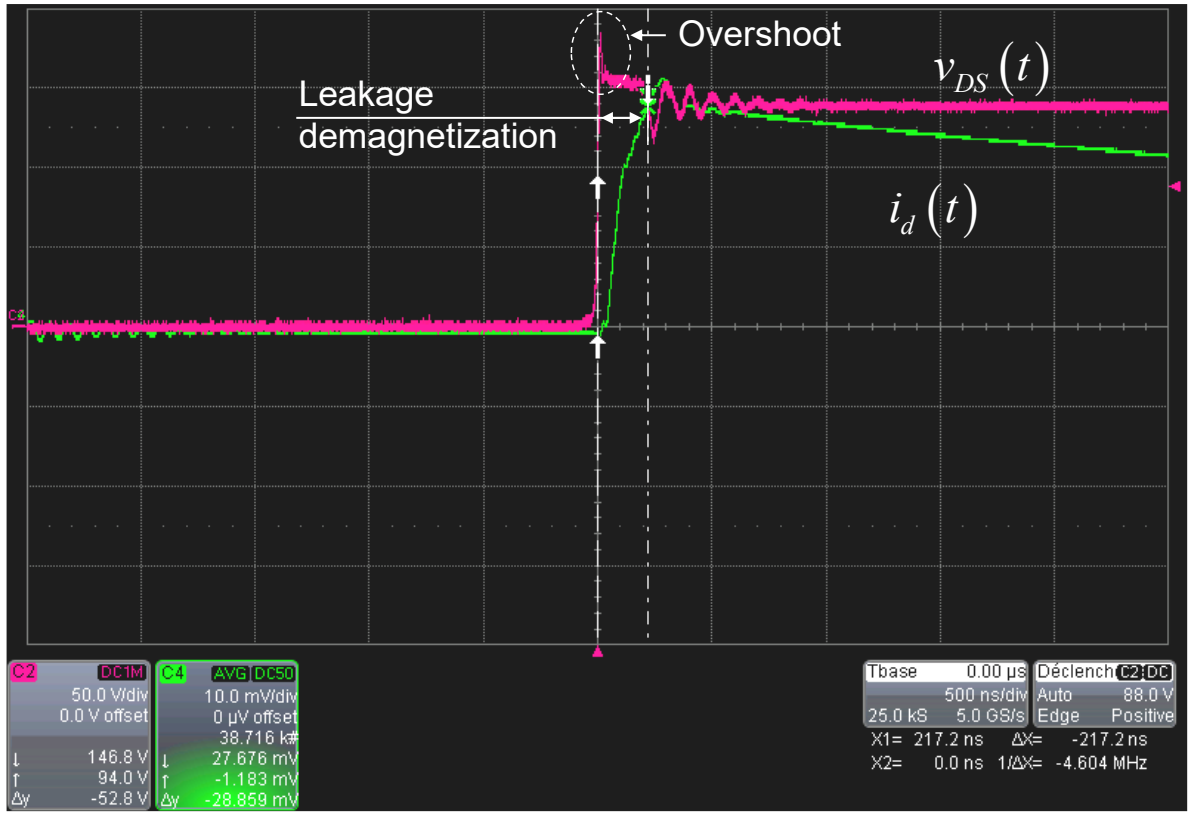


- The small-signal analysis reveals a quality factor Q dependent on l_{leak}
- Bode plot confirms damping action as leakage inductance increases

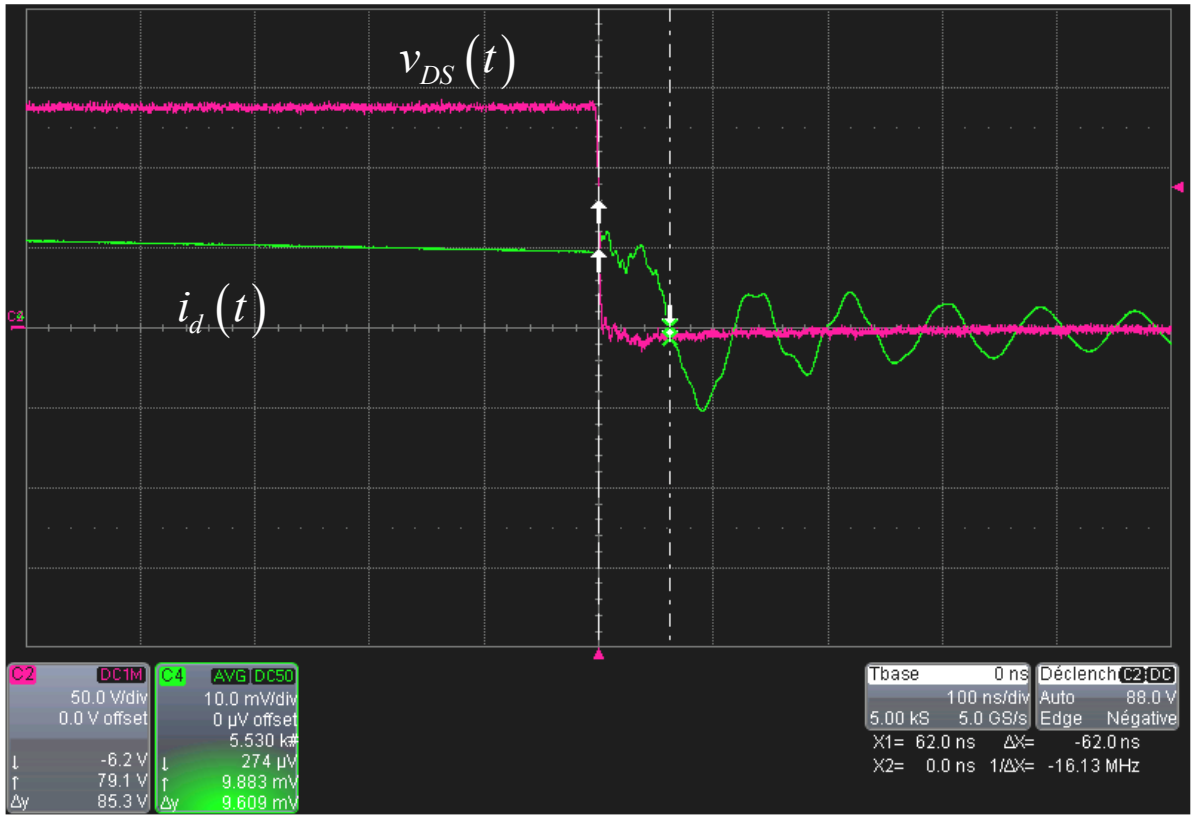


Measurements Waveforms

- Observing currents and voltages show the effects of the leakage inductance
- The small plateau on the drain indicates the clamp action until l_{leak} demagnetizes

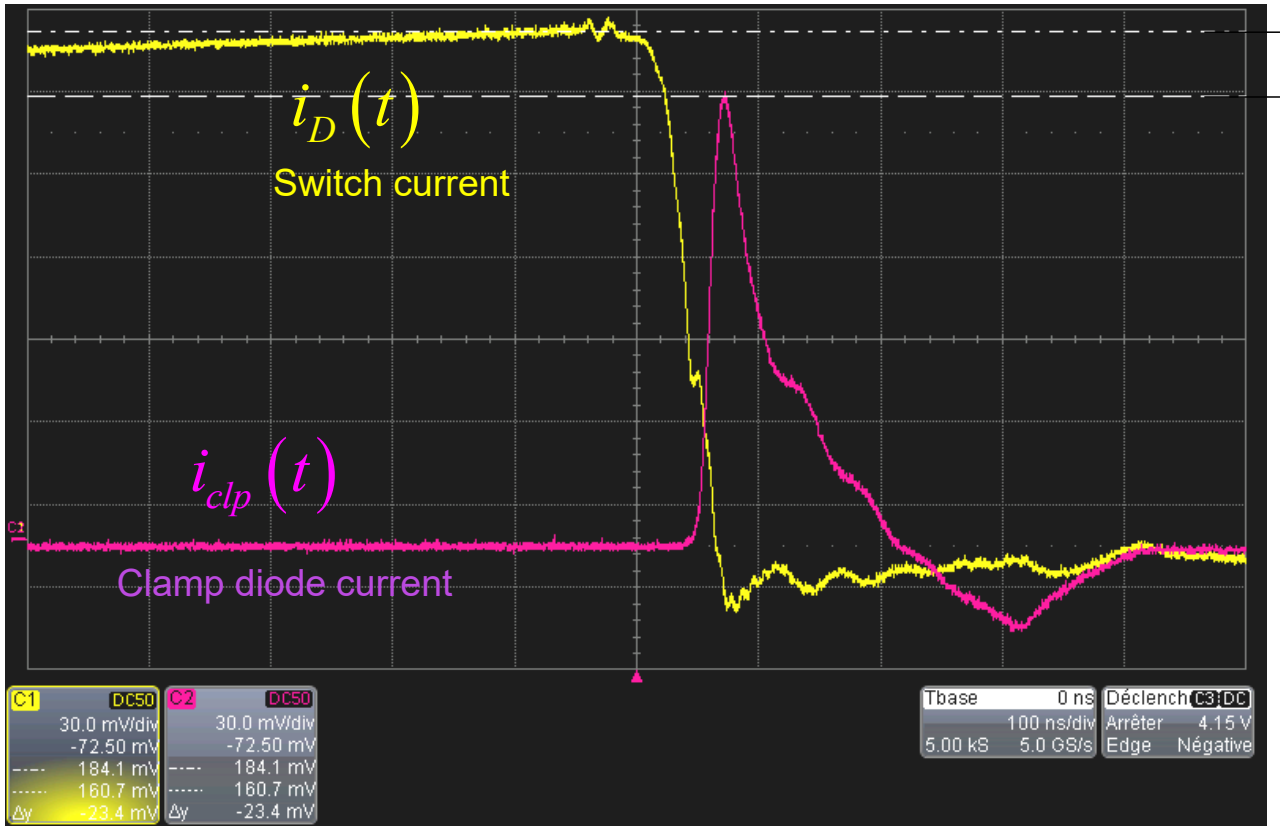


The drain is clamped by the RCD network but watch for the overshoot!



The output diode keeps conducting until the switch current rises from 0 to the valley I_v

Less Current in the RCD Clamp



- The capacitance lumped at the drain, requires energy to charge
- The charging process takes away some of the energy stored by the leakage and magnetizing inductance

✓ The current eventually flowing in the RCD clamp diode is reduced

✓ Dissipated power is reduced

$\Delta I = 240$ mA

$(0.240/1.84)*100 = 13\%$

Power is reduced by ≈**24.4%**

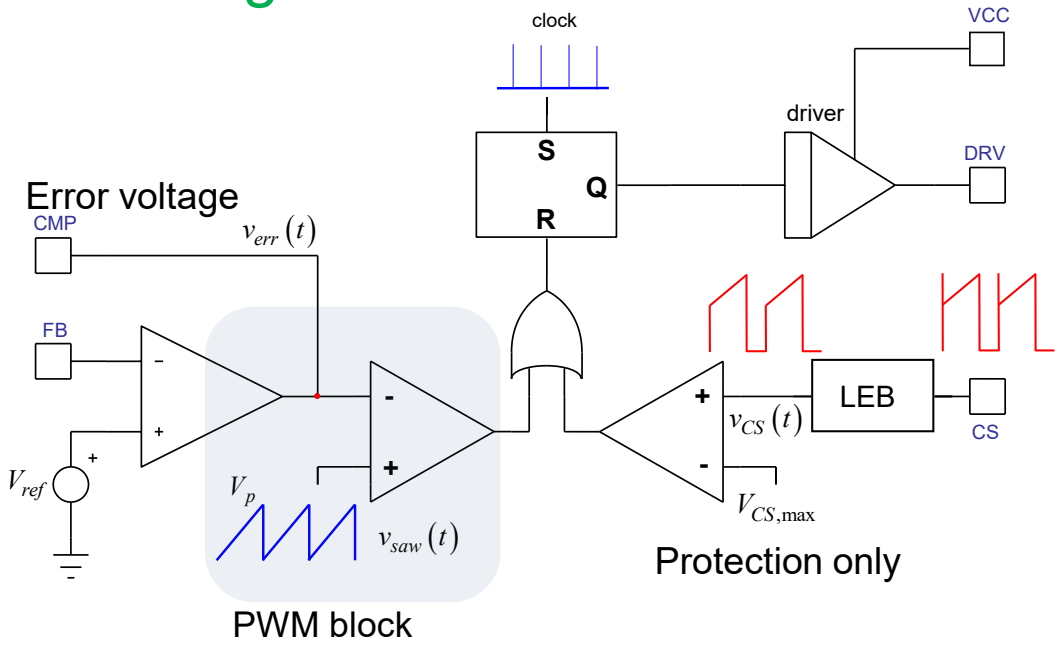
Agenda

- Theory of operation
- Controlling the Converter
- Current-Mode Instabilities
- The Right-Half-Plane Zero
- Closing the Loop with the Flyback Converter

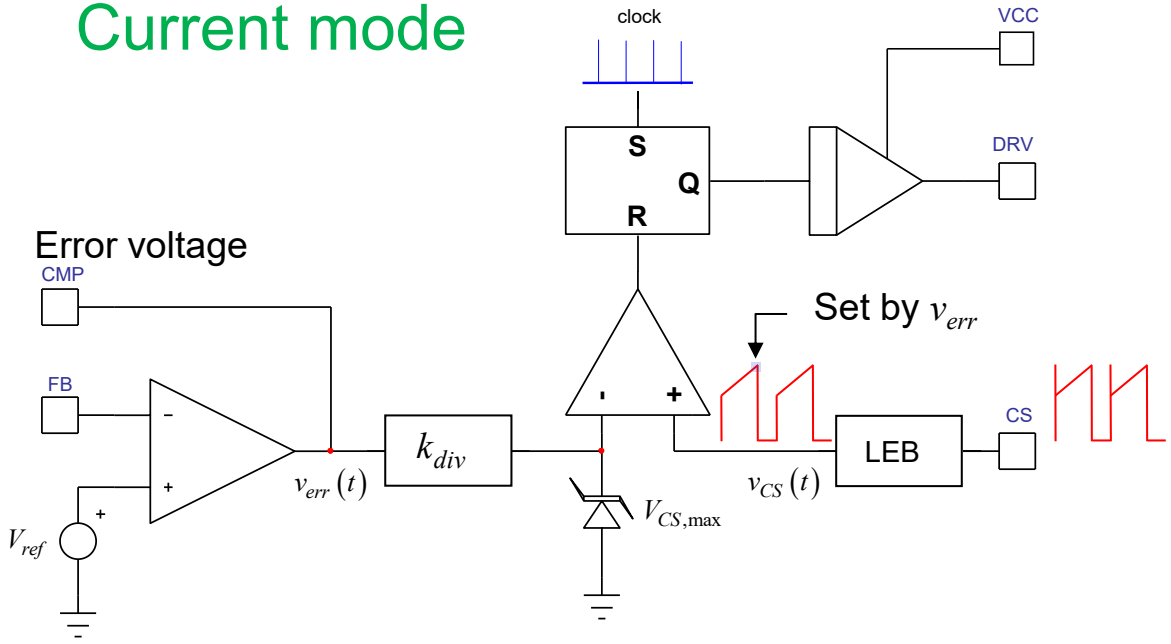
Voltage- or Current-Mode Control?

- A switching converter can be controlled in different ways
- The most classical solutions are fixed-frequency voltage- and current-mode control

Voltage mode



Current mode



- ✓ In VM control, the error voltage *directly* determines the duty ratio
- ✓ In CM control, the error voltage controls the peak current and *indirectly* the duty ratio

Which Control Technique is the best?

- Each control technique presents advantages and drawbacks

Voltage-mode control

- Ease of implementation: no need to sense inductor current
- Can operate down to very low duty ratio
- Large-amplitude artificial voltage brings good noise immunity
- Inherently-low output impedance
- ❖ Poor input rejection: any perturbation must first propagate before correction
- ❖ Variable second-order response complicates compensation

power integrations

many controllers from POWI operate in voltage-mode control

Current-mode control

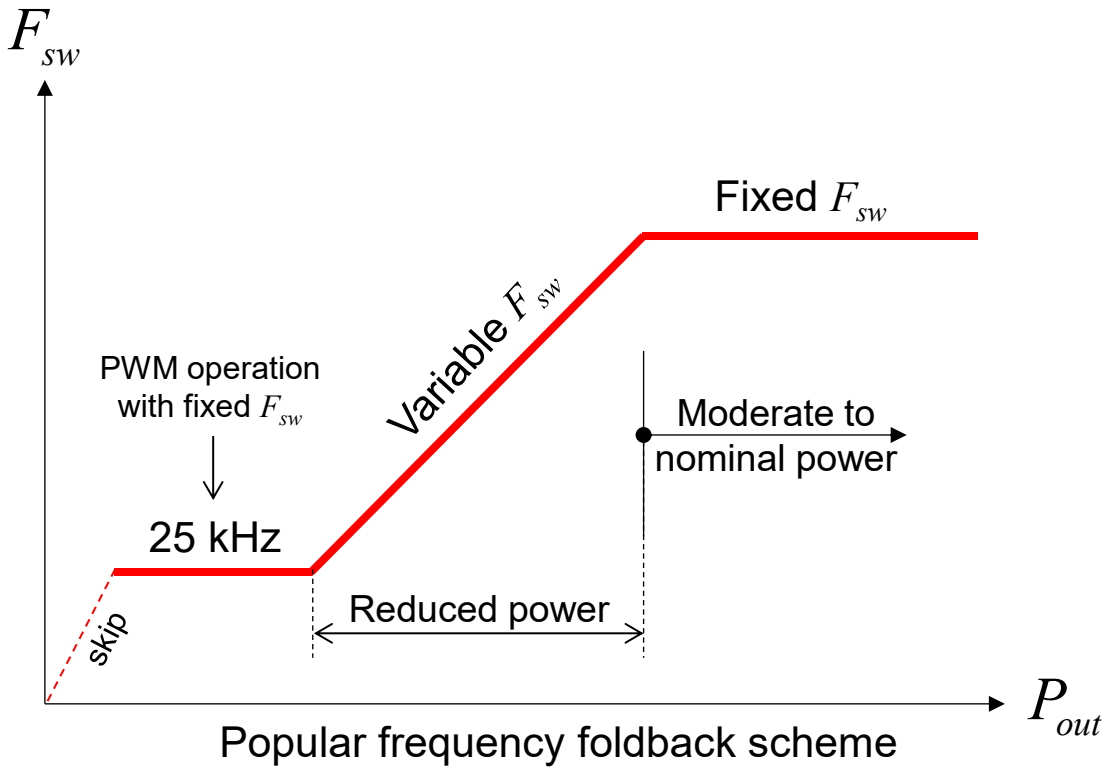
- Natural input feedforward brings excellent input voltage rejection
- Inherent cycle-by-cycle overcurrent protection
- First-order response eases feedback loop design
- ❖ Inherently-high output impedance requires high loop gain
- ❖ Sub-harmonic instability in CCM needs slope compensation
- ❖ Difficult to operate at very low duty ratio

onsemi NXP MPS

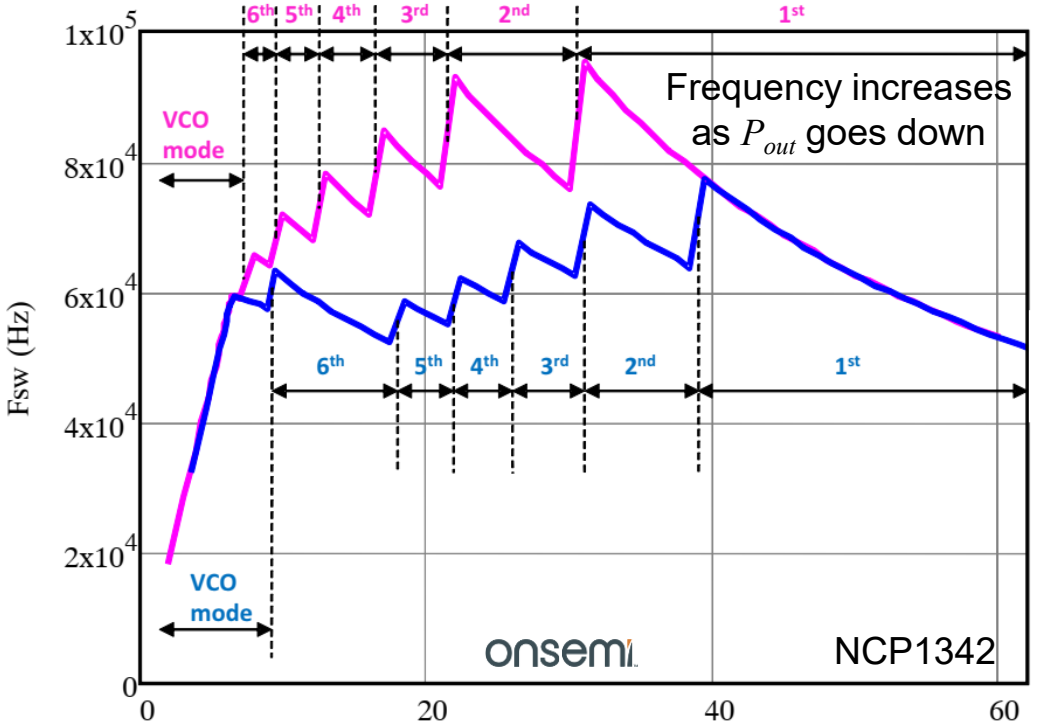
Mostly current-mode control

Various Control Schemes

- Fixed-frequency operation was the most popular approach years ago
- Trend towards lower standby power have propelled more efficient options



Popular frequency foldback scheme



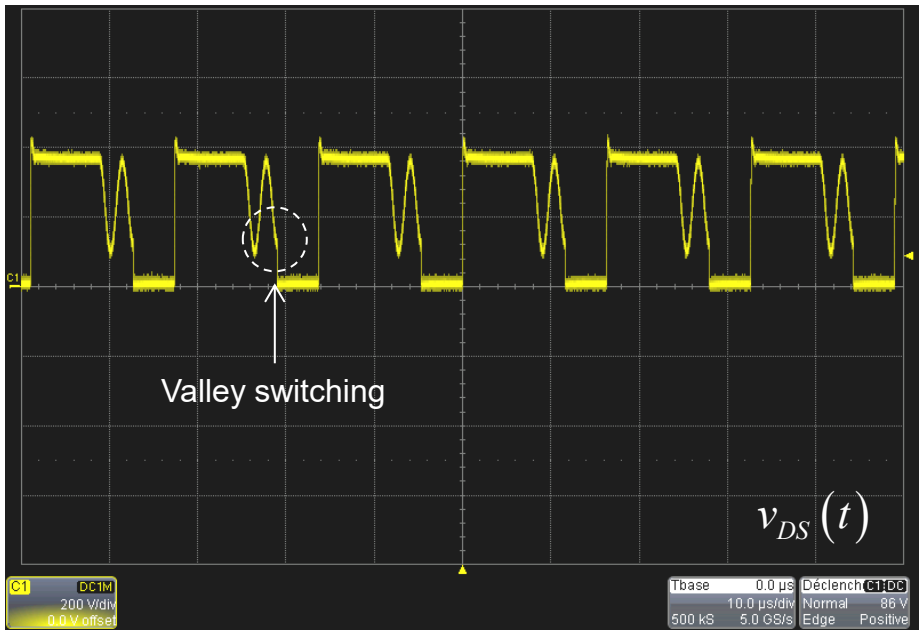
Quasi-resonant with valley lockout

- The frequency reduces in light-load conditions until skip-cycle is entered at no-load
- In QR, frequency increases until a VCO takes over and forces jumps in adjacent valleys

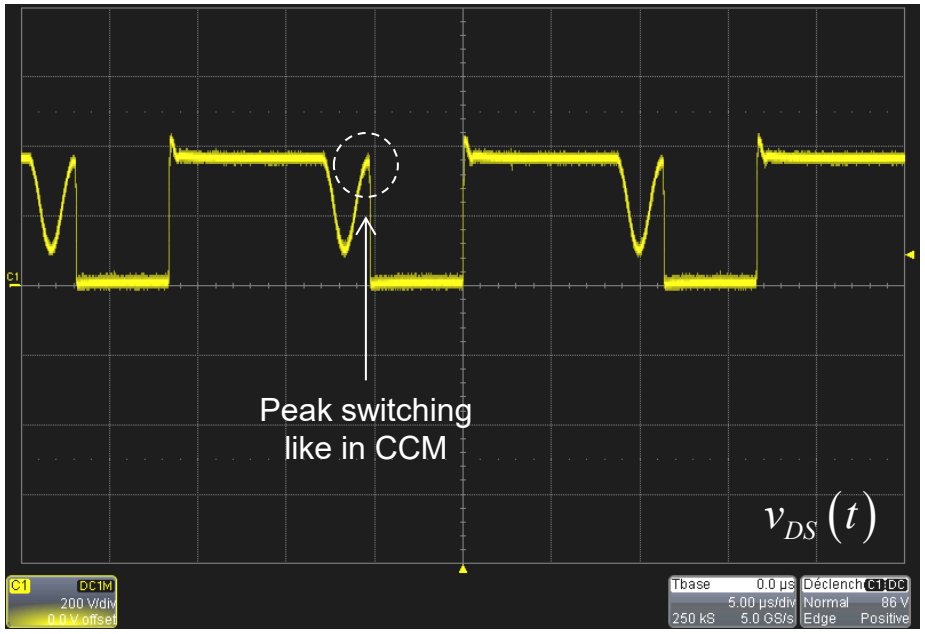
Hard-Switching versus Valley-Switching

- Asynchronous turn-on brings significant switching losses scaled by the frequency
- Quasi-resonance or QR allows valley-switching operation but frequency varies
- ✓ Multi-mode control is a good combination between CCM and DCM QR

Lucky



Unlucky



Lower loss

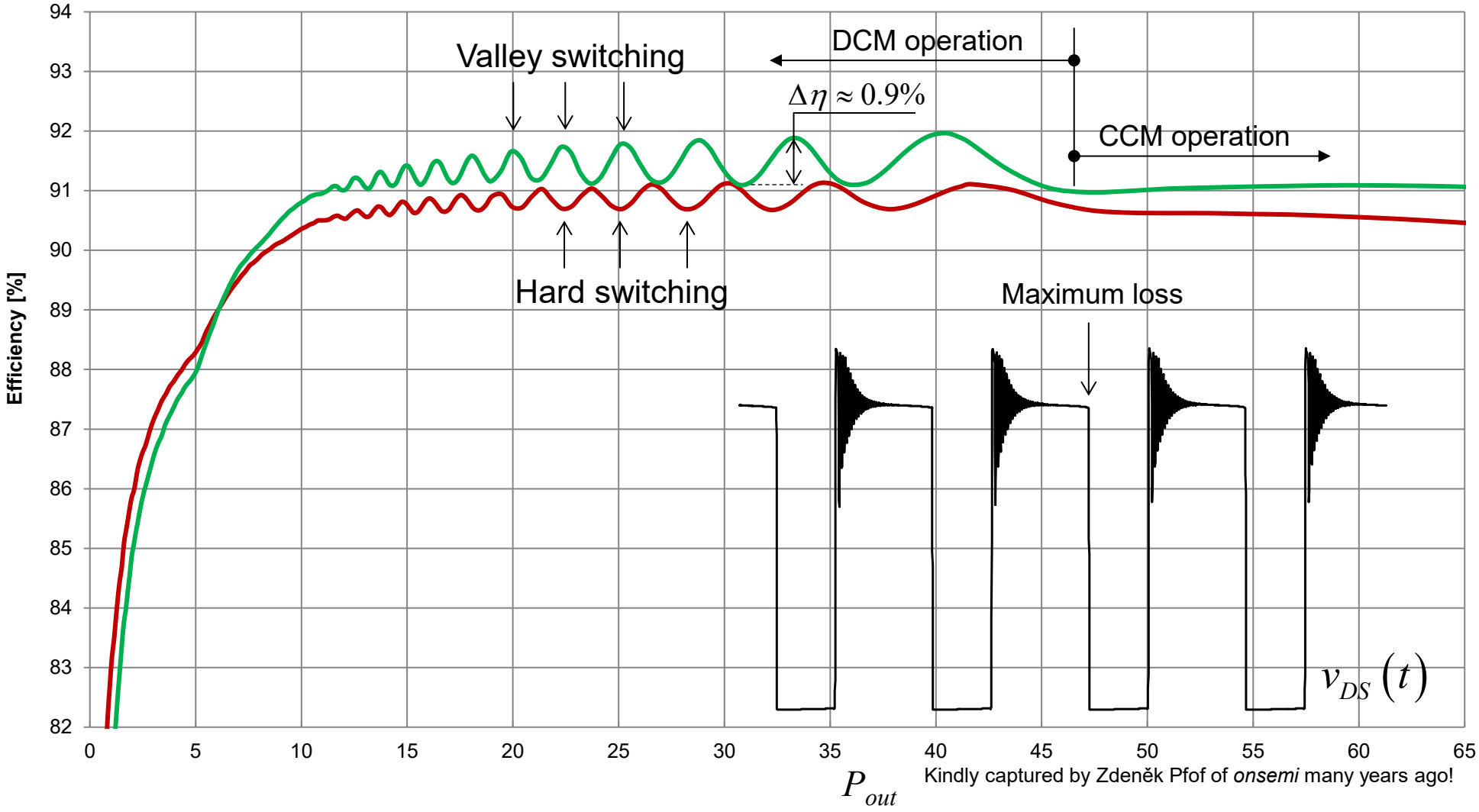
$$P_{sw} \approx 0.5 \cdot V_{DS}{}^{2} F_{sw} C_{lump}$$

nonlinear

Higher loss

Multimode Operation improves Efficiency

- Efficiency improves when valley-switching operation is enabled in DCM



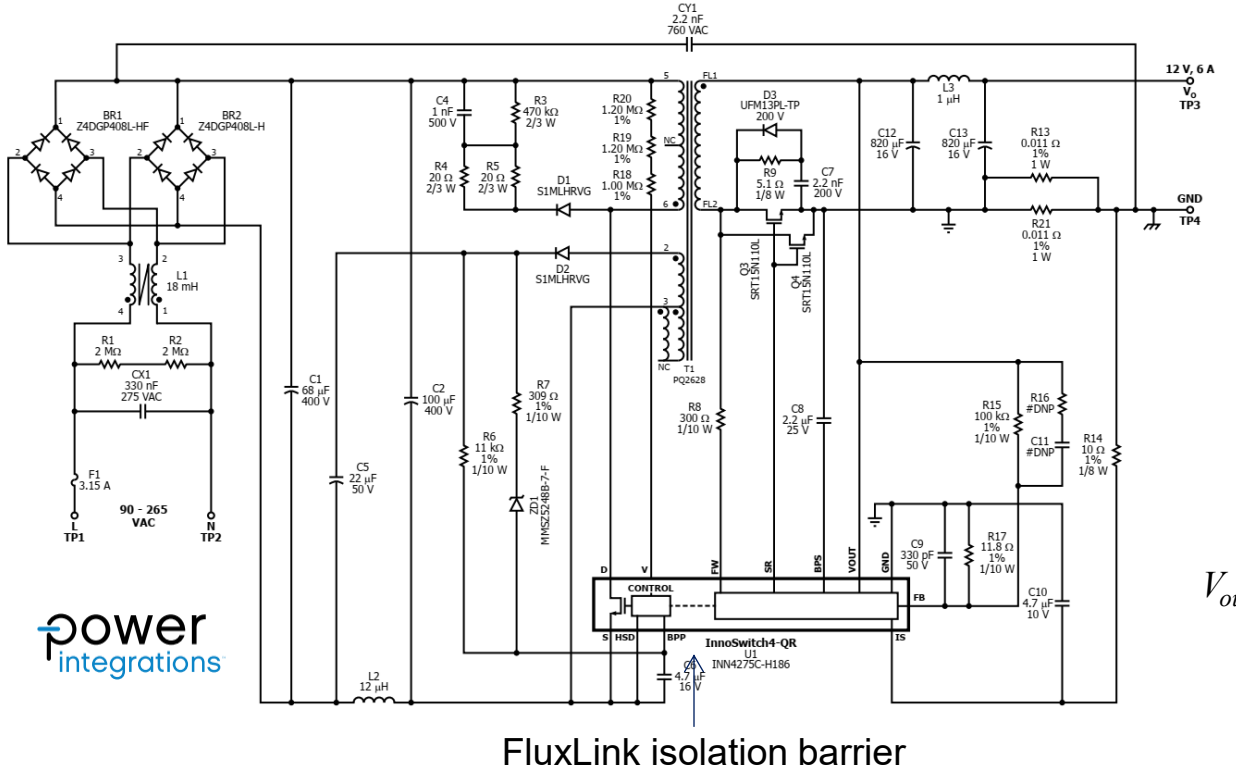
Kindly captured by Zdeněk Pfof of *onsemi* many years ago!

Good Riddance Optocoupler!

- The optocoupler brings galvanic isolation but hampers response time 
- Several options exist to remove this component while ensuring good regulation

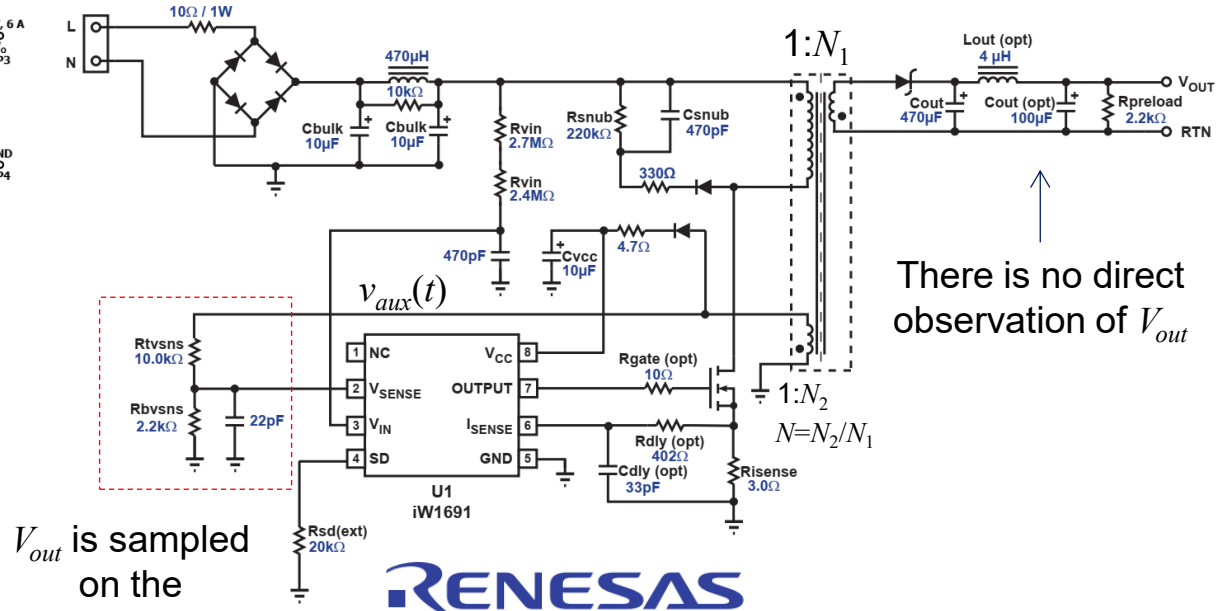
✓ Magnetic or capacitive coupling in the package

✓ Primary-side regulation or PSR



power integrations

FluxLink isolation barrier



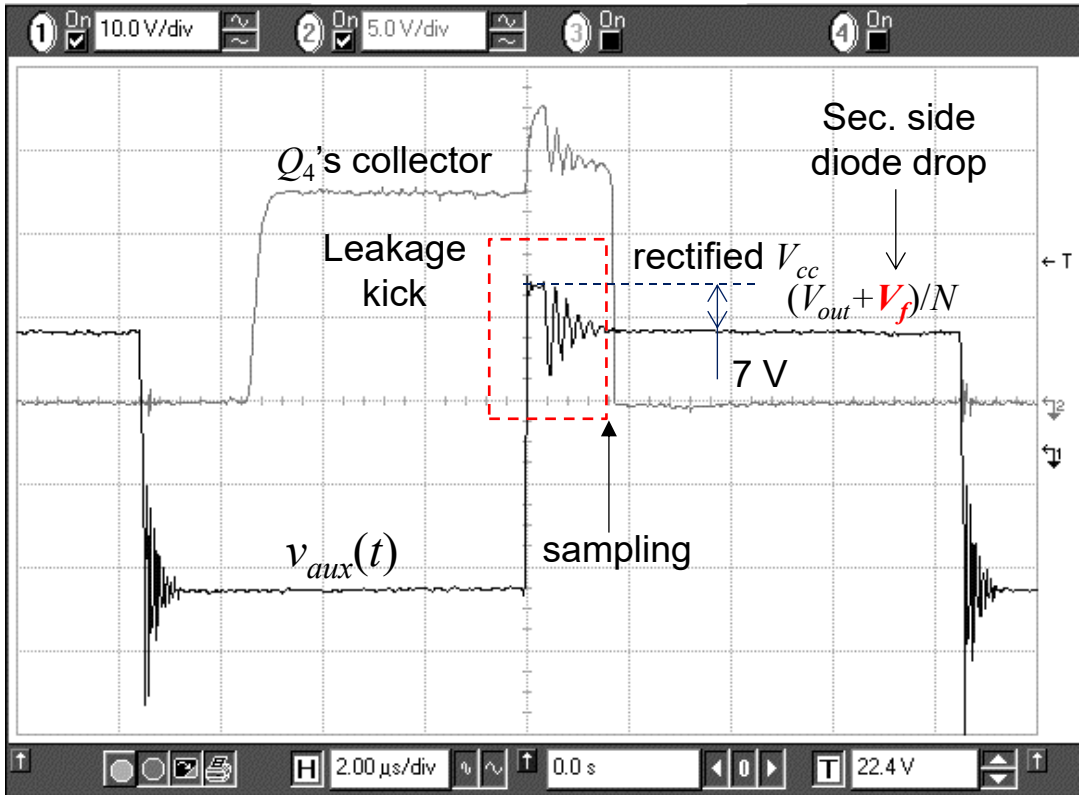
There is no direct observation of V_{out}

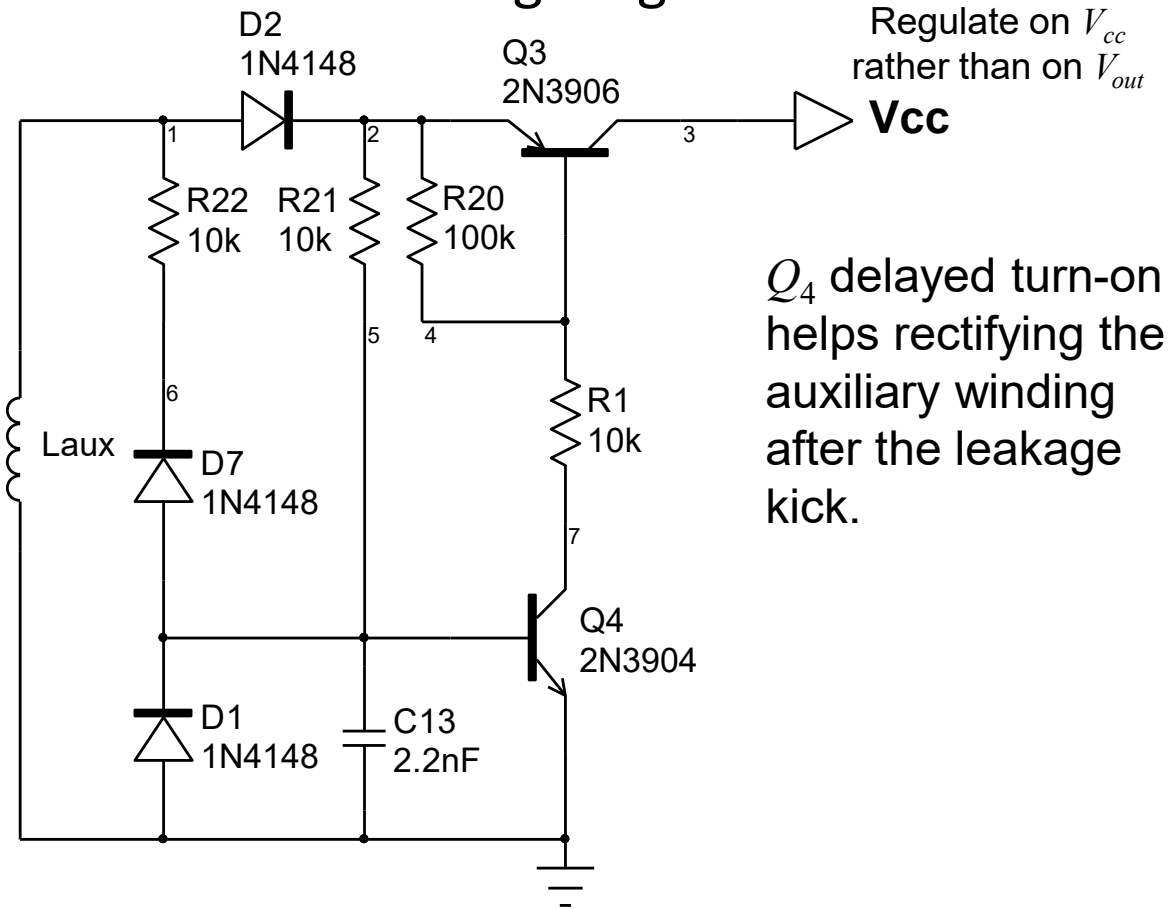
V_{out} is sampled on the auxiliary winding

RENESAS

Primary-Side Regulation – Cheap Version

- Observing the rectified auxiliary provides a means to regulate from the primary side
- Unfortunately, the leakage inductance affects the rectified voltage big time





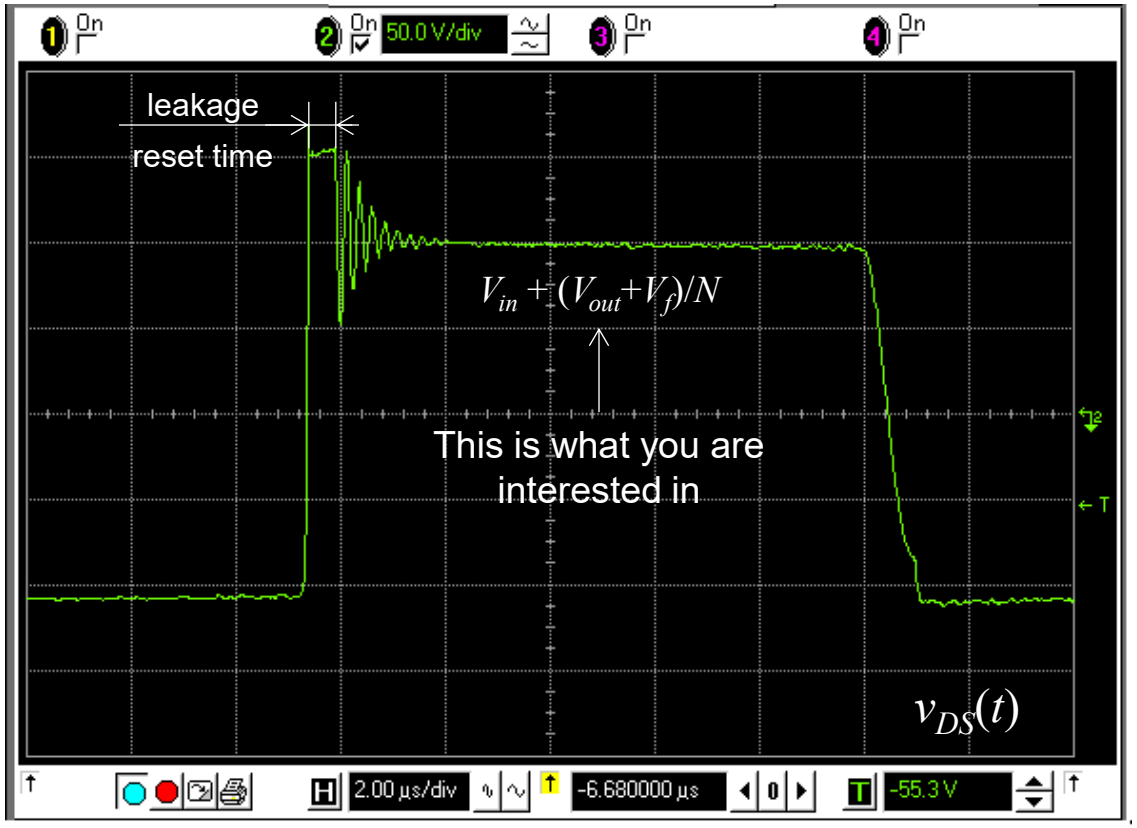
Q_4 delayed turn-on helps rectifying the auxiliary winding after the leakage kick.

✓ This simple circuit delays the voltage acquisition and can be used for regulation purposes

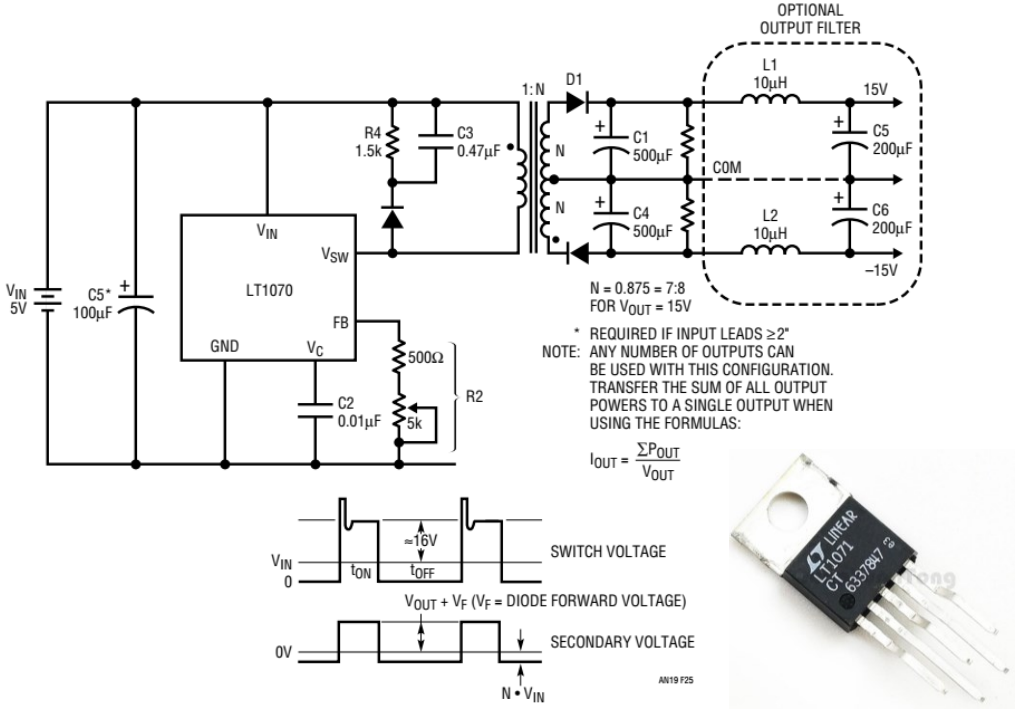
C. Basso, *Transistors tame Perfidious Leakage Inductance*, EDN Design Ideas, September 27th, 2001

Sensing the Drain Voltage

- The drain voltage swings to the reflected output voltage during the off-time
- ✓ If you subtract the input voltage contribution, you have access to V_{out}
- ✓ If you average the drain voltage, you also can approximate the input voltage V_{in}



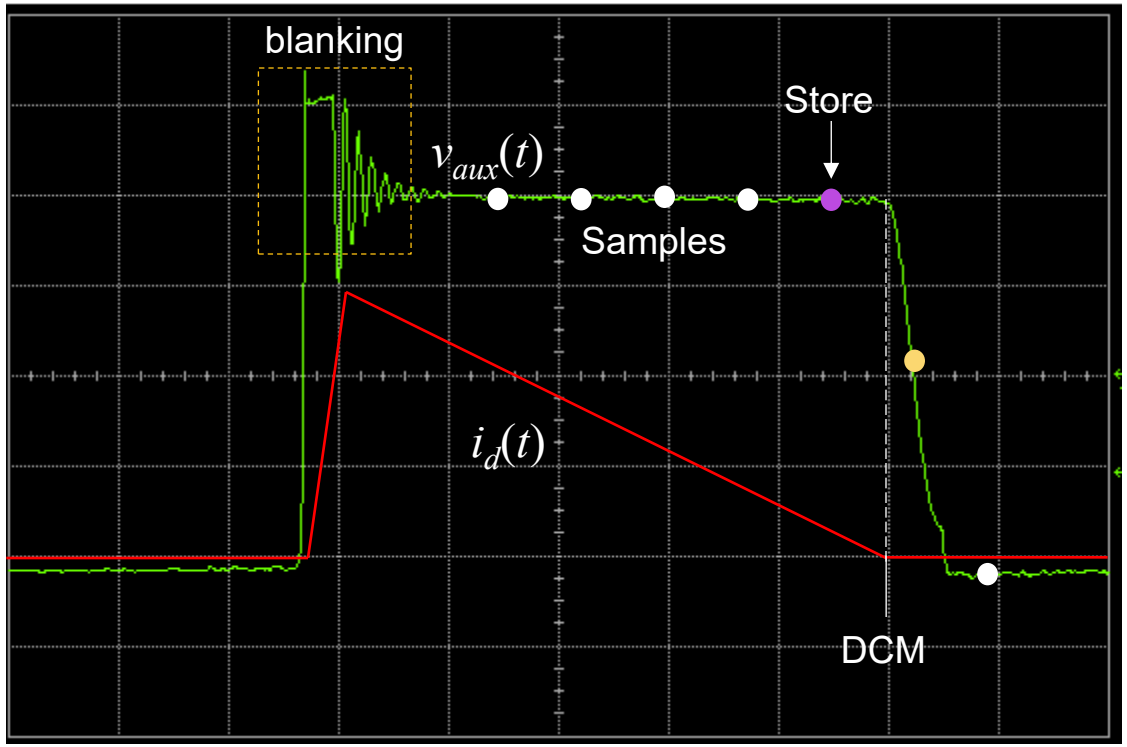
- This approach was adopted by the popular LT1070 from Linear Technology and released in the 80s.
- ❖ A low-voltage auxiliary winding is nowadays used



Primary-Side Regulation – Modern Version

- The leakage inductance plays a role in the sampled voltage: blanking is important
- The secondary diode forward drop is also involved: its V_f depends on I_{out}

✓ Detect the diode blocking event and sample the voltage prior to complete turn-off



Error

$$V_{aux} = (V_{out} + V_f)/N$$

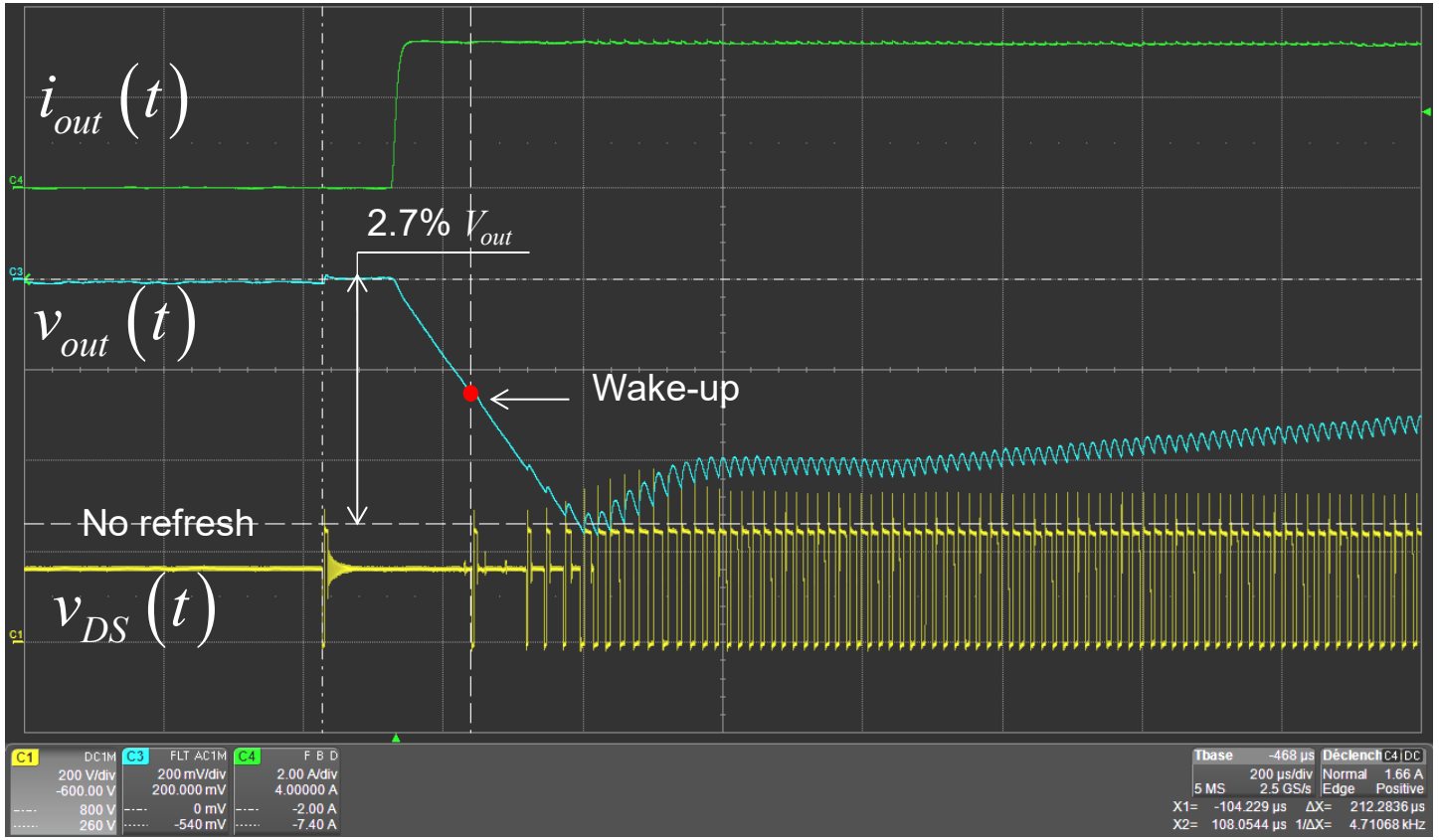
- The output diode forward drop is the smallest when its current is zero
- Sample the auxiliary voltage and detect when the last sample brings a low value: DCM is entered
- Go back to the *antepenultimate* sample and store the value

✓ You have a clean reconstructed V_{out}, free of leakage and forward drop errors

A Wake-Up Call is Needed!

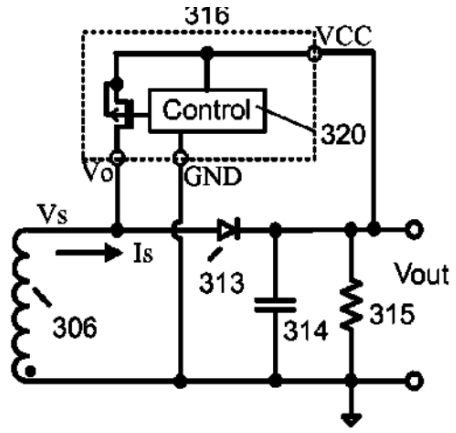
- The output voltage is only sampled after a turn-on event
- The controller is blind to any change on V_{out} occurring between two cycles

❖ How to regulate at a low switching frequency and ensure good transient response?



- In standby mode, the switching period can be as high as 1 ms
- Any event occurring within 1 ms is ignored
- You need to wake the controller up in case V_{out} drops

✓ A brief short-circuit across the output diode is sensed on the primary side

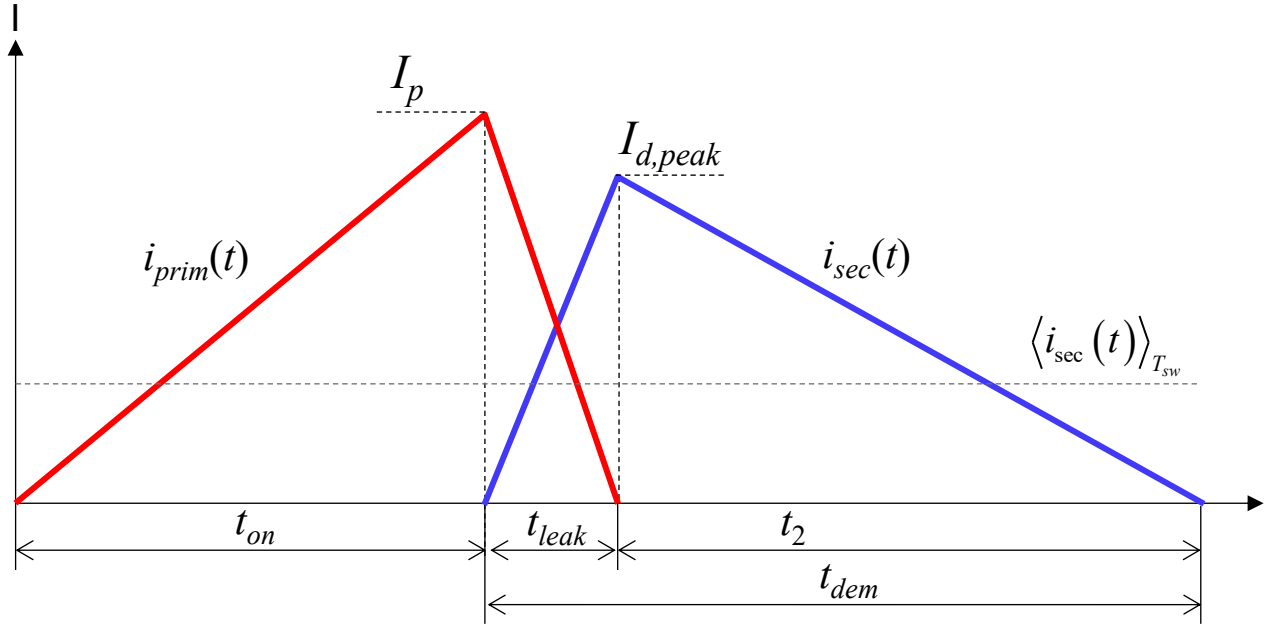


US 8,125,799 B2
Feb. 28, 2012

This technique was patented by BCD Shanghai Micro Electronics 8,125,199

Constant-Current Regulation

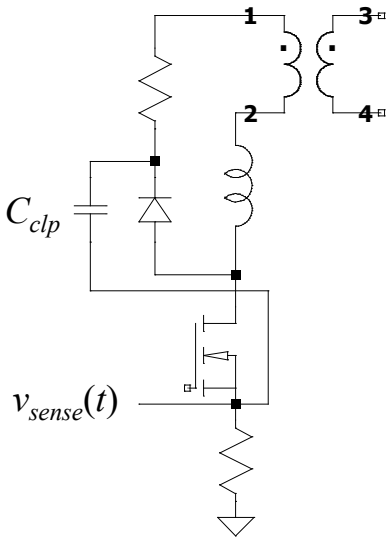
- Constant-voltage regulation is obtained by sampling the auxiliary plateau
- Constant-current relies on the primary peak current but depends on l_{leak}

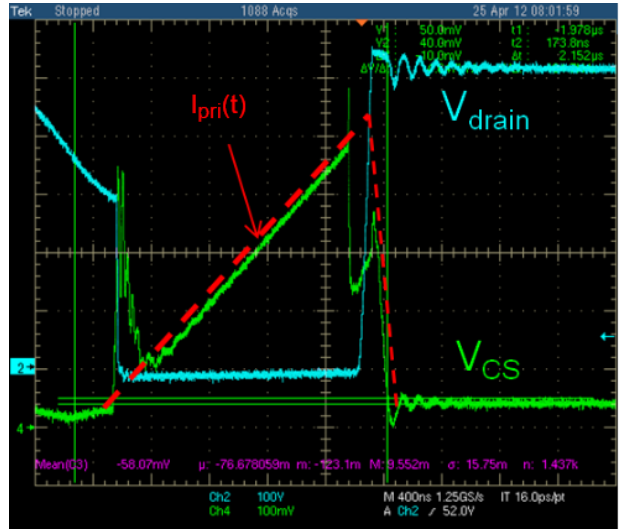


$$I_{d,peak} = \frac{I_{peak}}{N}\left(1 - \frac{l_{leak}}{L_p}\frac{1}{\frac{NV_{clp}}{V_{out}+V_f} - 1}\right) \Rightarrow I_{out} = I_{d,peak}\frac{t_{dem}}{2T_{sw}}$$

- Route the clamp capacitor to the sense pin for estimating the leakage reset time

✓ The control senses the delayed zeroing of $v_{sense}(t)$





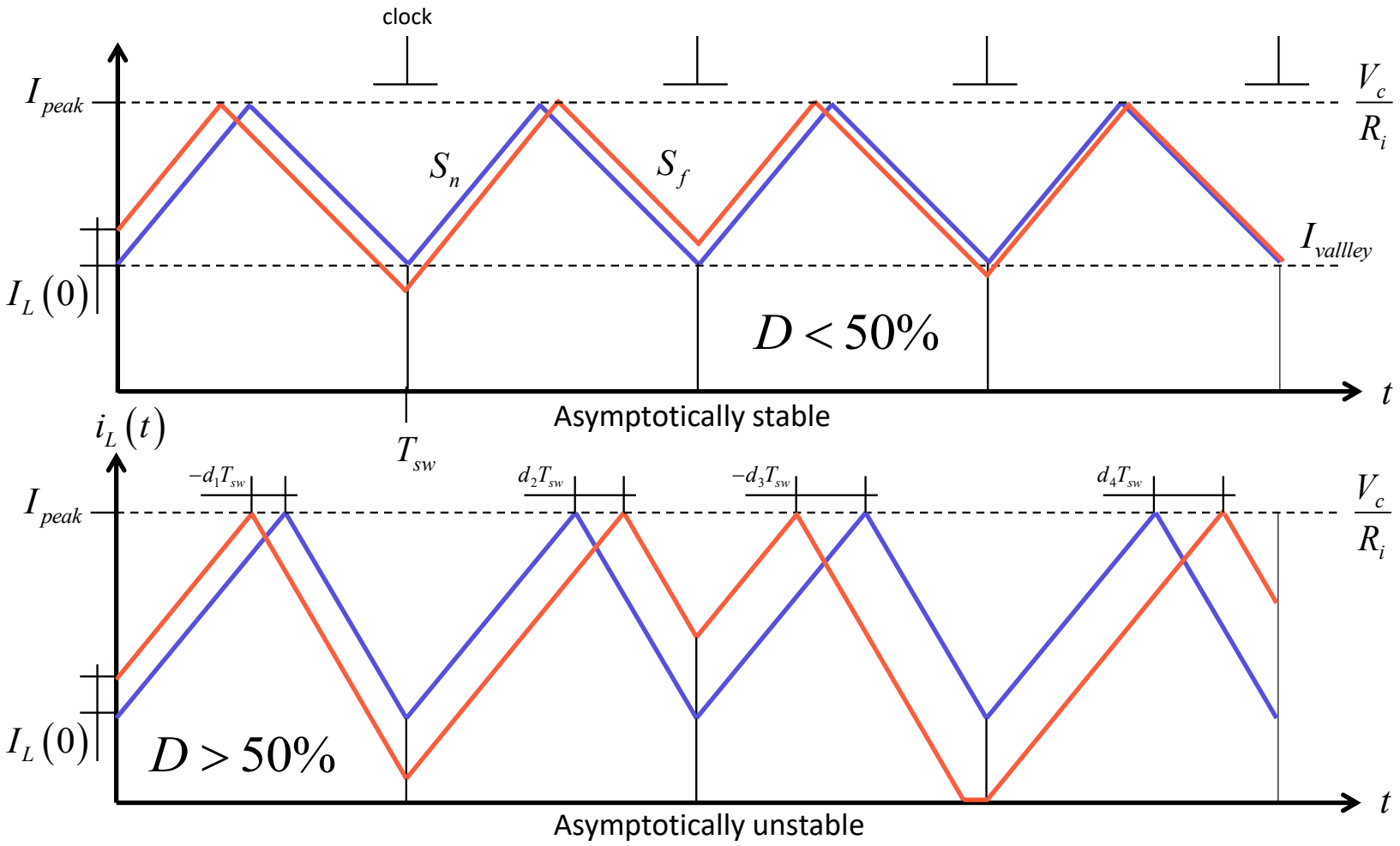
Agenda

- Theory of operation
- Controlling the Converter
- Current-Mode Instabilities
- The Right-Half-Plane Zero
- Closing the Loop with the Flyback Converter

Instability in the Inductor Current

- The current loop of a converter can be prone to instabilities in certain conditions

✓ If the power supply operates in CCM with a duty ratio exceeding 50%, it can oscillate



- The perturbation ΔI_L propagates cycle-by-cycle and obeys the below expression:

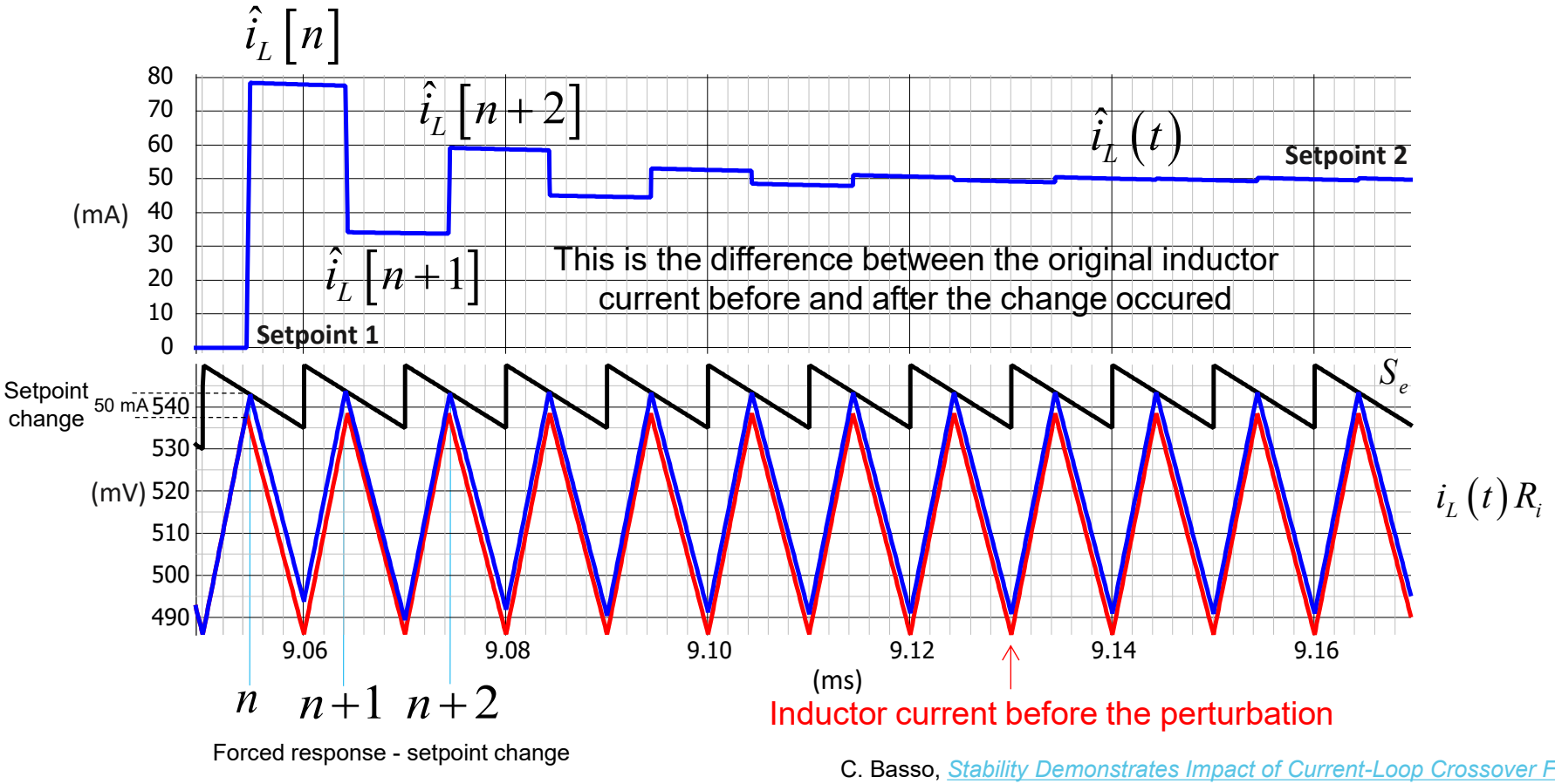
$$\Delta I_L\left(nT_{sw}\right) = \Delta I_L\left(0\right)\left(-\frac{D}{D'}\right)^n$$

- When D remains below 50%, the response is oscillatory but damped: the perturbation dies out in a few cycles.

- When D exceeds 50%, the system becomes chaotic and produces subharmonic oscillations at $F_{sw}/2$.

An Oscillatory Response to a Change

- The current loop samples and holds the inductor peak current, cycle-by-cycle
- This phenomenon affects the ac response of the current loop
- ✓ Characterizing the current loop is essential to ensure stability of the converter



Forced response - setpoint change

- In this picture, you can see in red the steady-state inductor current
- The control asks for a 50-mA change in the peak current setpoint
- The sampling event occurs when the peak intersects the compensation ramp S_e
- The inductor peak current slightly overshoots then stabilizes after 6-7 switching cycles

C. Basso, *Stability Demonstrates Impact of Current-Loop Crossover Frequency on Stability*, How2Power, January 2021

Sampled Data Analysis with Z-Transform

FUTURE ELECTRONICS
A WT Microelectronics Company

- The current loop analysis involves discrete values like D and the inductor peak current
- We must derive the relationship linking V_c to $I_{L,peak}$ for characterizing the current loop
- ✓ The *total* response is the sum of the *natural* and *forced* responses: $y(t) = r_n(t) + r_f(t)$

natural forced

Natural response: $\hat{i}_L[n+1] = -\alpha \cdot \hat{i}_L[n]$ This is the response to a perturbation in the inductor current, e.g. V_{in} step

Forced response: $\hat{i}_L[n+1] = \frac{1}{R_i}(1+\alpha) \cdot \hat{v}_c[n+1]$ This is the response to a change in the control voltage, V_c

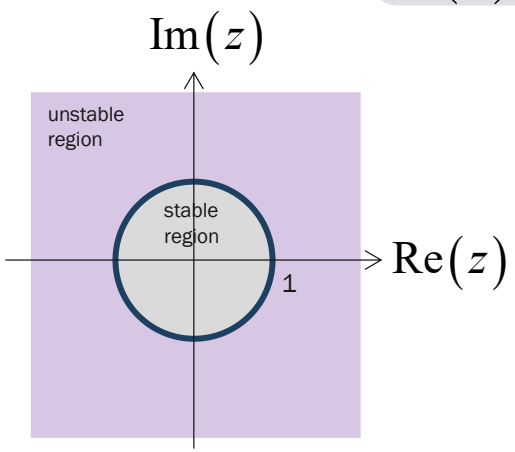
Combine equations
Involve z-transform

$$\frac{\hat{i}_L(z)}{\hat{v}_c(z)} = \frac{1}{R_i}(1+\alpha) \cdot \frac{z}{\alpha + z}$$

$$z_p = -\alpha$$

$$\alpha = \frac{S_f - S_e'}{S_n + S_e'}$$

S_f is the inductor downslope
S_n is the inductor current upslope
S'_e is the compensation ramp



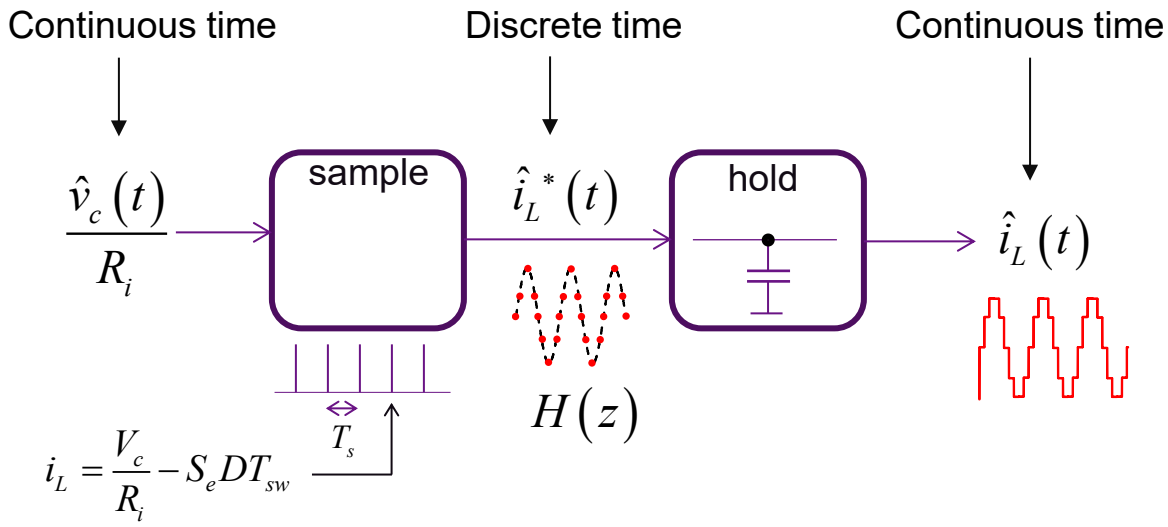
- The pole must remain within the unity circle for stability
- This is defined by $|\alpha| < 1$
- This is respected if $S_f < S_n$

$$\frac{V_{out}}{L} < \frac{V_{in} - V_{out}}{L} \Rightarrow D < 50\%$$

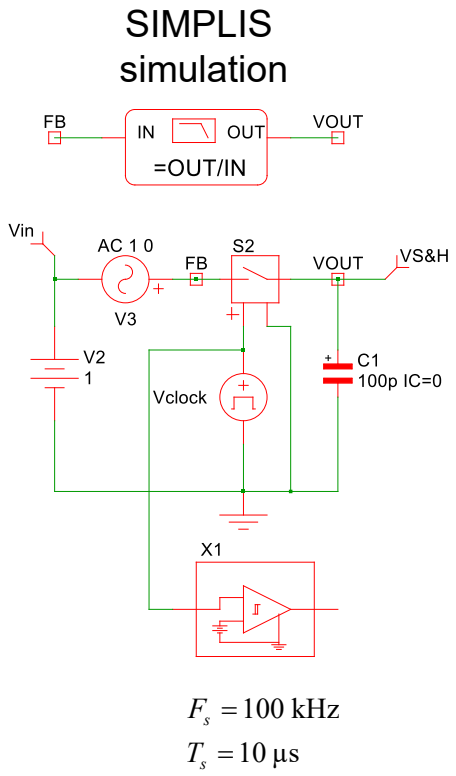
R. B. Ridley, *A new small-signal model for current-mode control*, PhD. dissertation, Virginia Polytechnic Institute and State University, 1990.

Accounting for the Sample & Hold Effect

- The current loop involves discrete values: the duty ratio and the inductor peak current
- The whole process is analogous to a sample and hold chain and introduces a ZOH
- ✓ It can be characterized with sampled data analysis

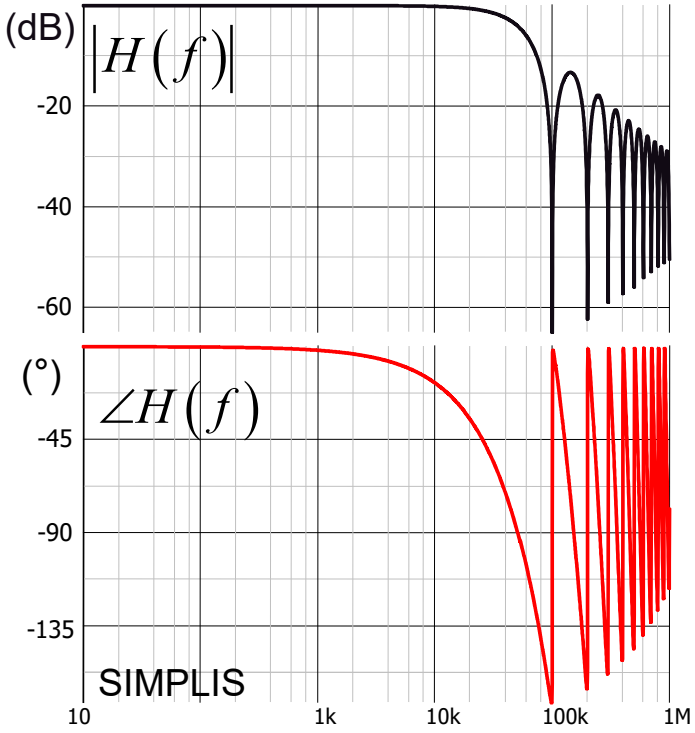


Zero-Order Hold ⇒ $H(s) = \frac{1 - e^{-sT_s}}{sT_s}$



$F_s = 100\ \text{kHz}$

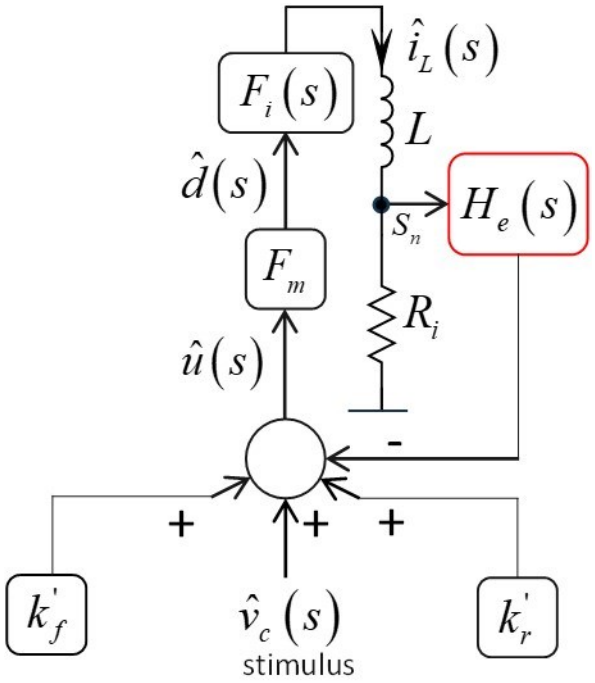
$T_s = 10\ \mu\text{s}$

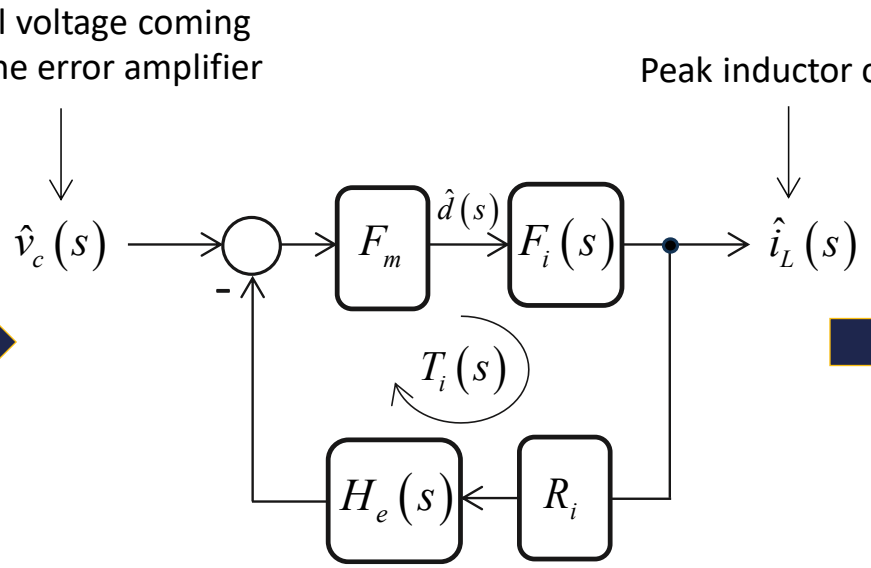


Current Loop in the Frequency Domain

- The final transfer function in the Laplace-domain includes the ZOH expression
- It contains exponential terms that need to be approximated for easier manipulations
- ✓ We know that $z = e^{sT_s}$ to update the previous expression

$$F(s) = \frac{\hat{i}_L(s)}{\hat{v}_c(s)} = \frac{1}{R_i}(1+\alpha)\frac{e^{sT_s}}{e^{sT_s}+\alpha}\underbrace{\frac{1-e^{-sT_s}}{sT_s}}_{\text{ZOH}} = \frac{1}{R_i}(1+\alpha)\frac{1}{sT_s}\frac{e^{sT_s}-1}{e^{sT_s}+\alpha}$$





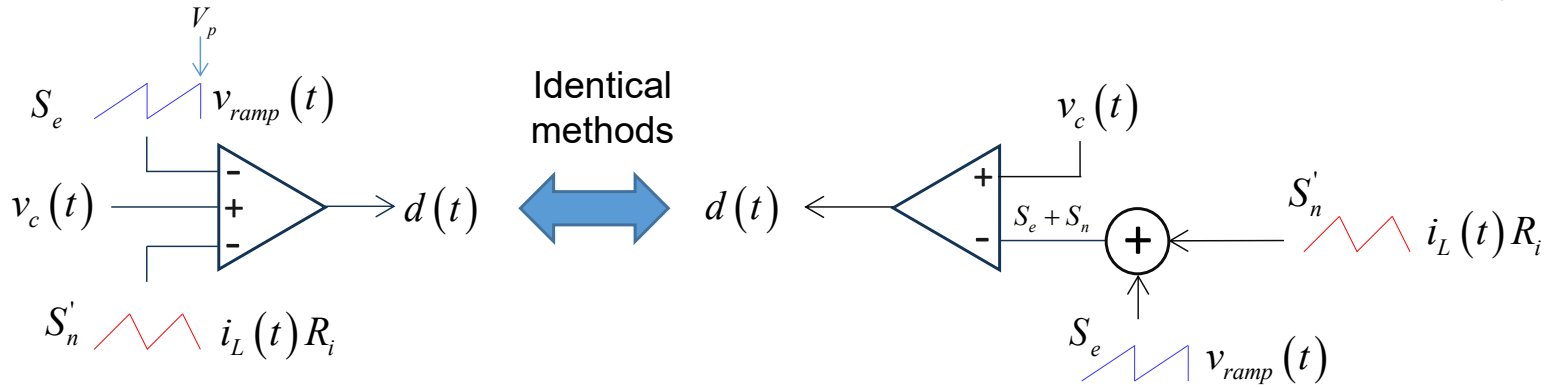
- This is the complete closed-loop transfer function linking the inductor peak current to the control voltage
- We already know that this expression is described by $F(s)$
- What is $H_e(s)$, the sampling effect?

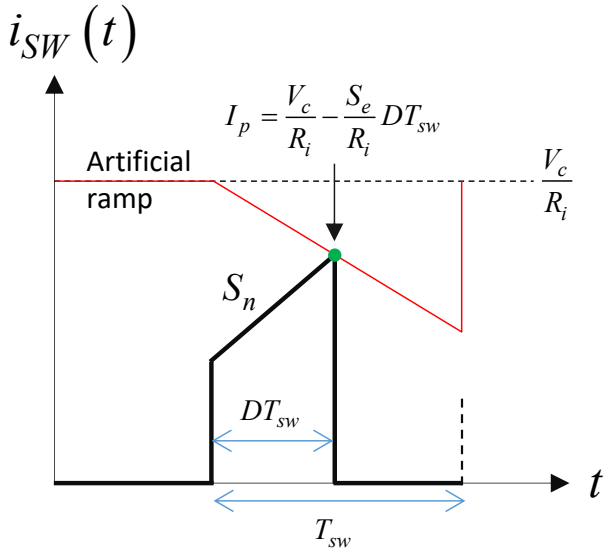
$$\frac{\hat{i}_L(s)}{\hat{v}_c(s)} = \frac{F_m F_i(s)}{1+F_m F_i(s) H_e(s) R_i}$$

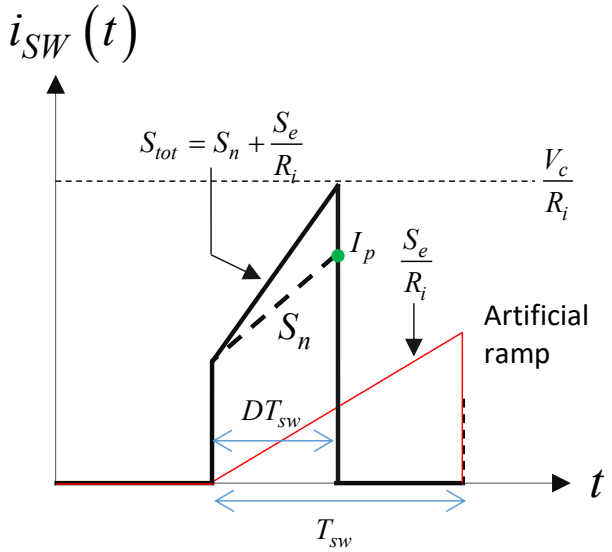
Need to determine the sampling block, $H_e(s)$

Determining the Unknown Expressions

- The closed-loop expression host three terms, F_m, F_i and H_e
- Each block should be determined to model the entire loop – we start with F_m





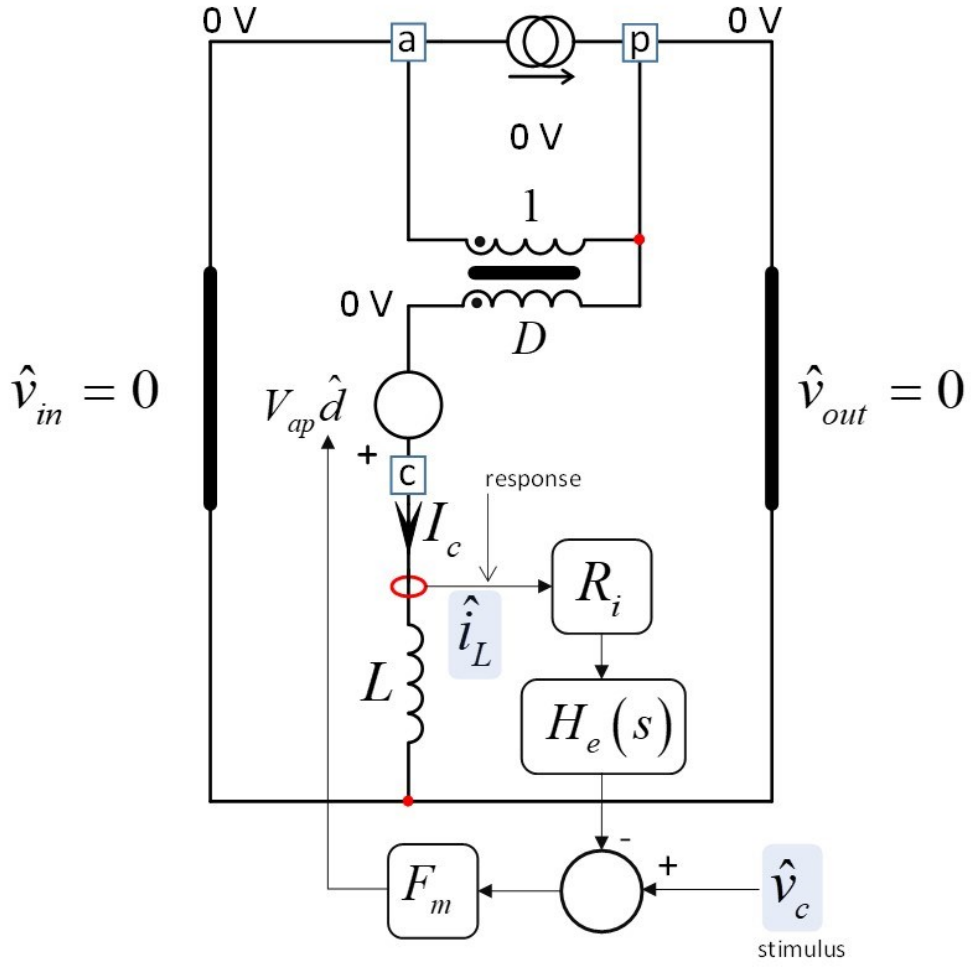


- The duty ratio modulator – the PWM block – receives the inductor current upslope S_n and the compensation ramp S_e
- The gain of the PWM block – F_m – involves the sum of the two slopes

$$F_m = \frac{D(s)}{V_c(s)} = \frac{1}{(S_e + S_n R_i) T_{sw}}$$

The Duty Ratio to Inductor Current Block

- The function block F_i links the duty ratio D to the inductor peak current I_L
- You need to invoke the PWM switch model with a few equations around it…



- The input and output voltages are zeroed considering v_c as the stimulus

$$I_L(s) = \frac{V_{ap} D(s)}{sL}$$

- Extract the link between I_L and D

$$\frac{I_L(s)}{D(s)} = F_i(s) = \frac{V_{ap}}{sL}$$

- Develop $V_{ap} = V_{ac} + V_{cp}$

$$\frac{V_{ap}}{sL} = \frac{V_{ac}}{sL} + \frac{V_{cp}}{sL}$$

- Express on and off slopes

$$S_n = \frac{V_{ac}}{L} \qquad S_f = \frac{V_{cp}}{L}$$

- Factor the expression

$$F_i(s) = \frac{S_n + S_f}{s}$$

We can now determine $H_e(s)$ having F_m and F_i on hand

Modeling the Sampling Block H_e

- Extracting $H_e(s)$ from the time-continuous expression is straightforward
- The definition still involves an exponential term which is difficult to handle

$$\frac{F_m F_i(s)}{1+F_m F_i(s) H_e(s) R_i} = \frac{1}{R_i}(1+\alpha)\frac{1}{sT_s}\frac{e^{sT_s}-1}{e^{sT_s}+\alpha} \quad \Rightarrow \quad H_e(s) = \frac{sT_s}{e^{sT_s}-1}$$

- The second-order Padé approximant is used to replace the exponential term

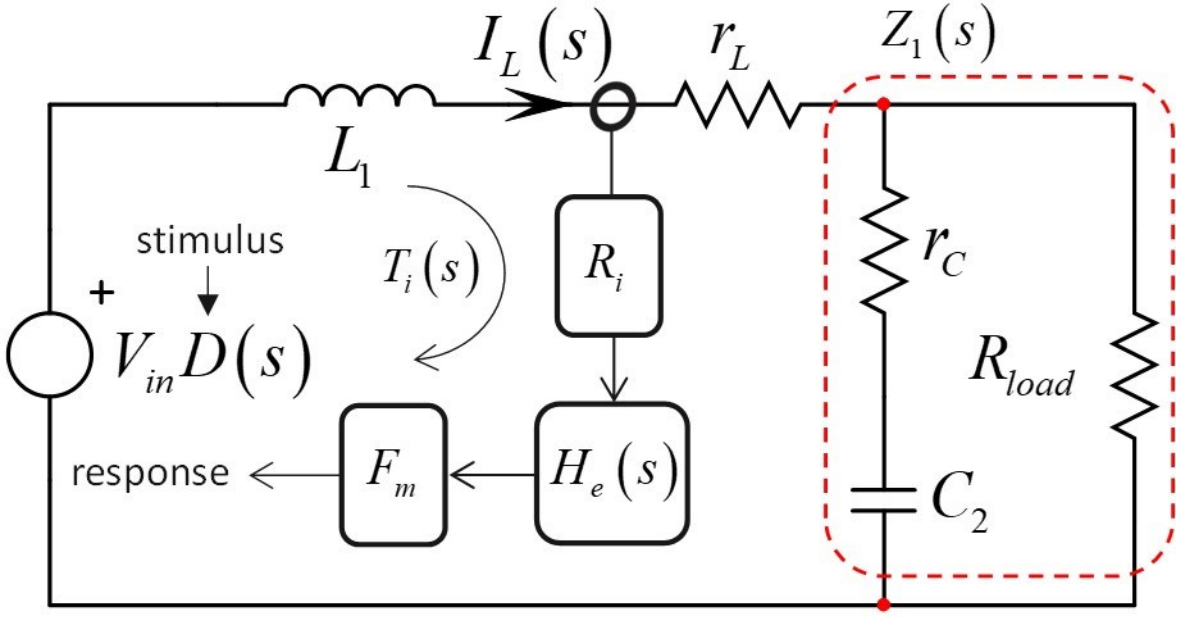
$$e^{sT_s} \approx \frac{1+\frac{1}{2/\pi}\left(\frac{s}{\omega_s/2}\right)+\left(\frac{s}{\omega_s/2}\right)^2}{1-\frac{1}{2/\pi}\left(\frac{s}{\omega_s/2}\right)+\left(\frac{s}{\omega_s/2}\right)^2} \quad \Rightarrow \quad H_e(s) \approx 1-\frac{s}{\omega_s/\pi}+\left(\frac{s}{\omega_s/2}\right)^2 = 1+\frac{s}{\omega_n Q}+\left(\frac{s}{\omega_n}\right)^2$$

$$Q = -\frac{2}{\pi} \qquad \omega_n = \frac{\omega_s}{2}$$

✓ The negative sign implies a pair of right-half-plane zeroes located at $F_{sw}/2$

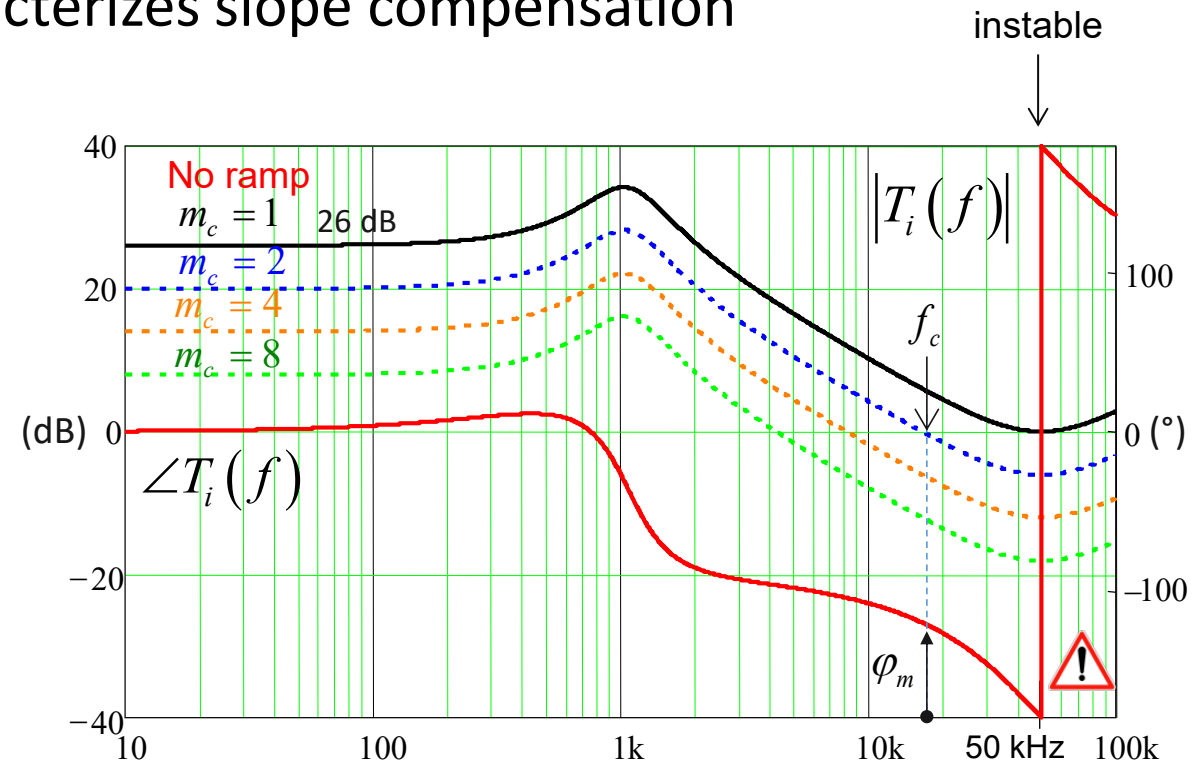
Plotting the Inner Current Loop Response

- We can now extract the current loop frequency response involving the load
- The loop gain T_i depends on m_c which characterizes slope compensation



$$T_i(s) \approx \frac{L_1}{R_{load} T_s m_c (1-D)} \frac{1 + sR_{load}C_2}{1 + \frac{s}{\omega_0 Q} + \left(\frac{s}{\omega_0}\right)^2} H_e(s)$$

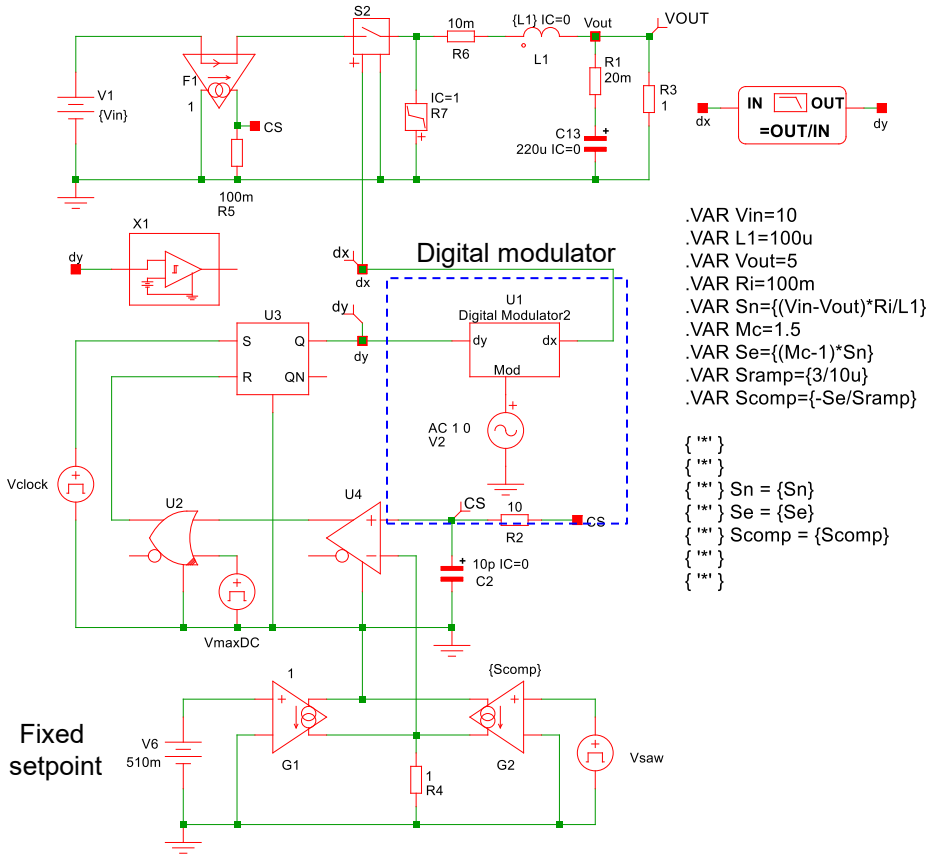
$$m_c = 1 + \frac{S_e'}{S_n}$$ compensation slope / on-time slope

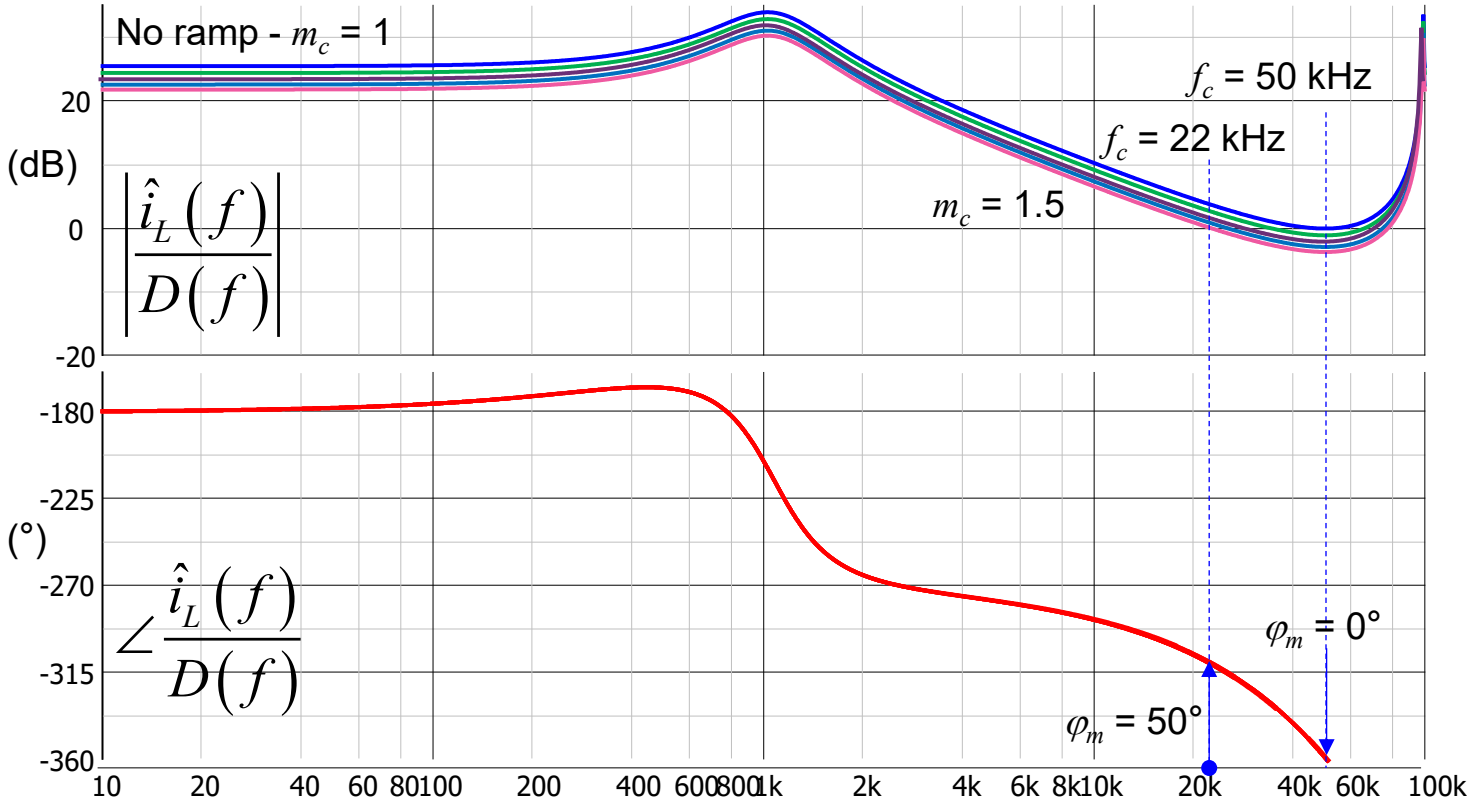


- ❖ The subharmonic instability arises because the current loop crossover is too high and suffers from the RHPZ pair which hampers phase margin
- ✓ Force a lower crossover with slope compensation

Measuring the Current Loop with SIMPLIS

- It is not necessary to measure the current loop when designing a converter
- It is however interesting to look at the current-loop response with a digital modulator



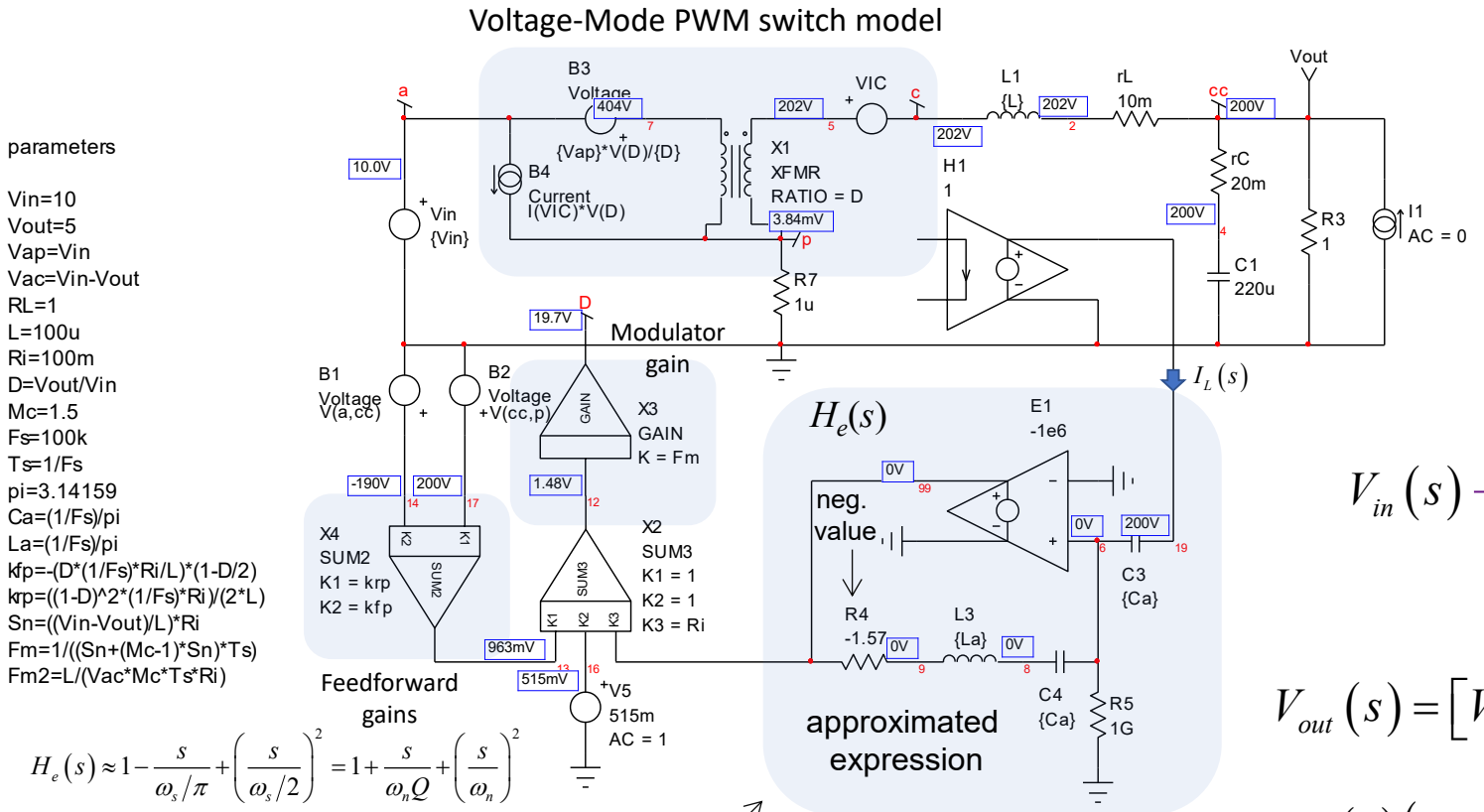


- The loop is measured without extra compensation ramp and is highly unstable
- Adding compensation ramp reduces the gain and forces crossover with a favorable phase margin (m_c = 1.5).

B. Cho, F. Lee, *Measurement of Loop Gain with the Digital Modulator*, IEEE Transactions on Power Electronics, January 1986

Revisiting the H_e Block

- In his original model, Ray Ridley did implement an active filter with two RHP zeroes
- This approximation leads to an excellent ac response between models and prototypes
- ✓ For learning purposes, why not trying the real sampled data expression in the model?



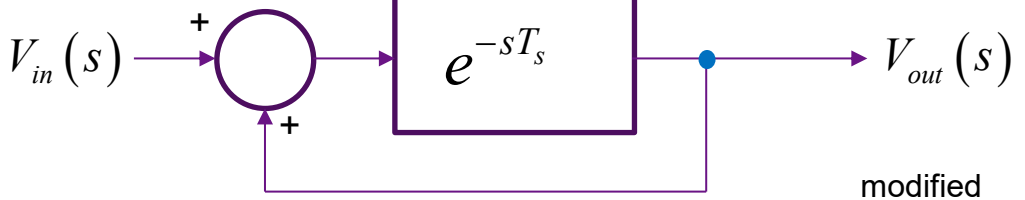
original expression

$$\frac{sT_s}{e^{sT_s}-1}\frac{e^{-sT_s}}{e^{-sT_s}} = \frac{e^{-sT_s}}{1-e^{-sT_s}}sT_s$$

modified expression

legendary DL470

Delay line



$$V_{out}(s) = \left[V_{out}(s) + V_{in}(s)\right]e^{-sT_s}$$

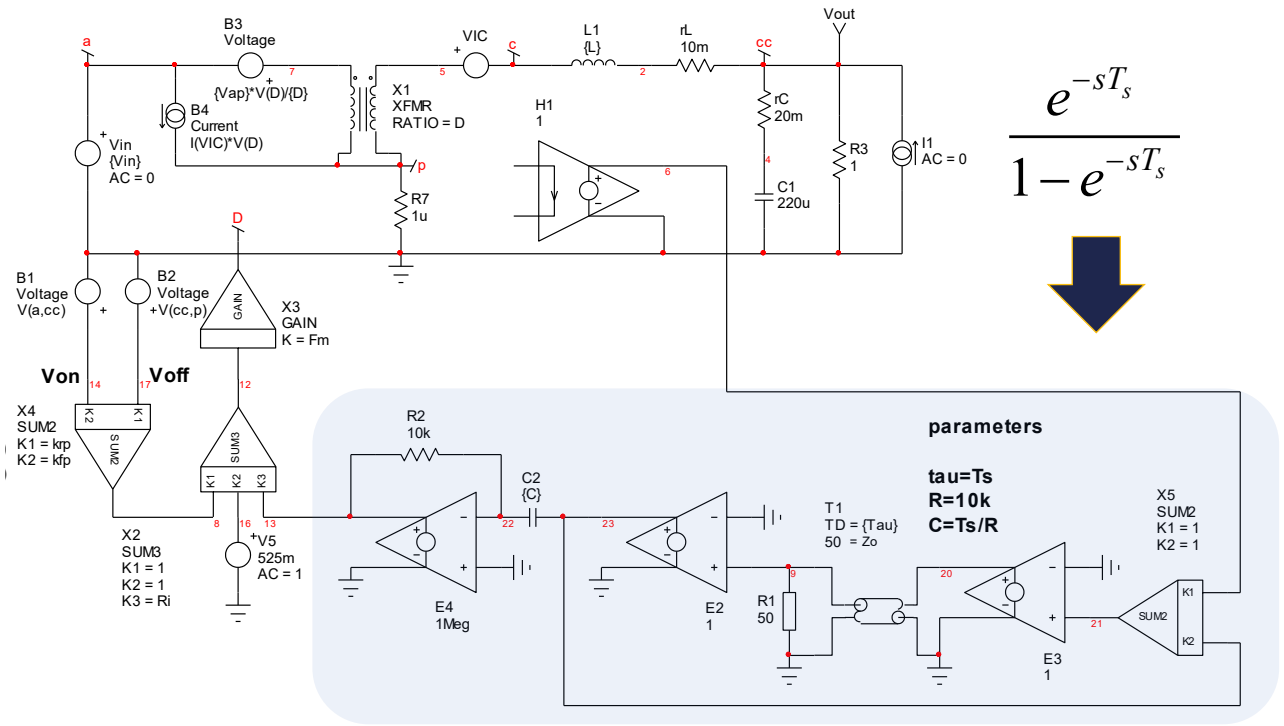
$$V_{out}(s)\left(1 - e^{-sT_s}\right) = V_{in}(s)e^{-sT_s}$$

modified expression

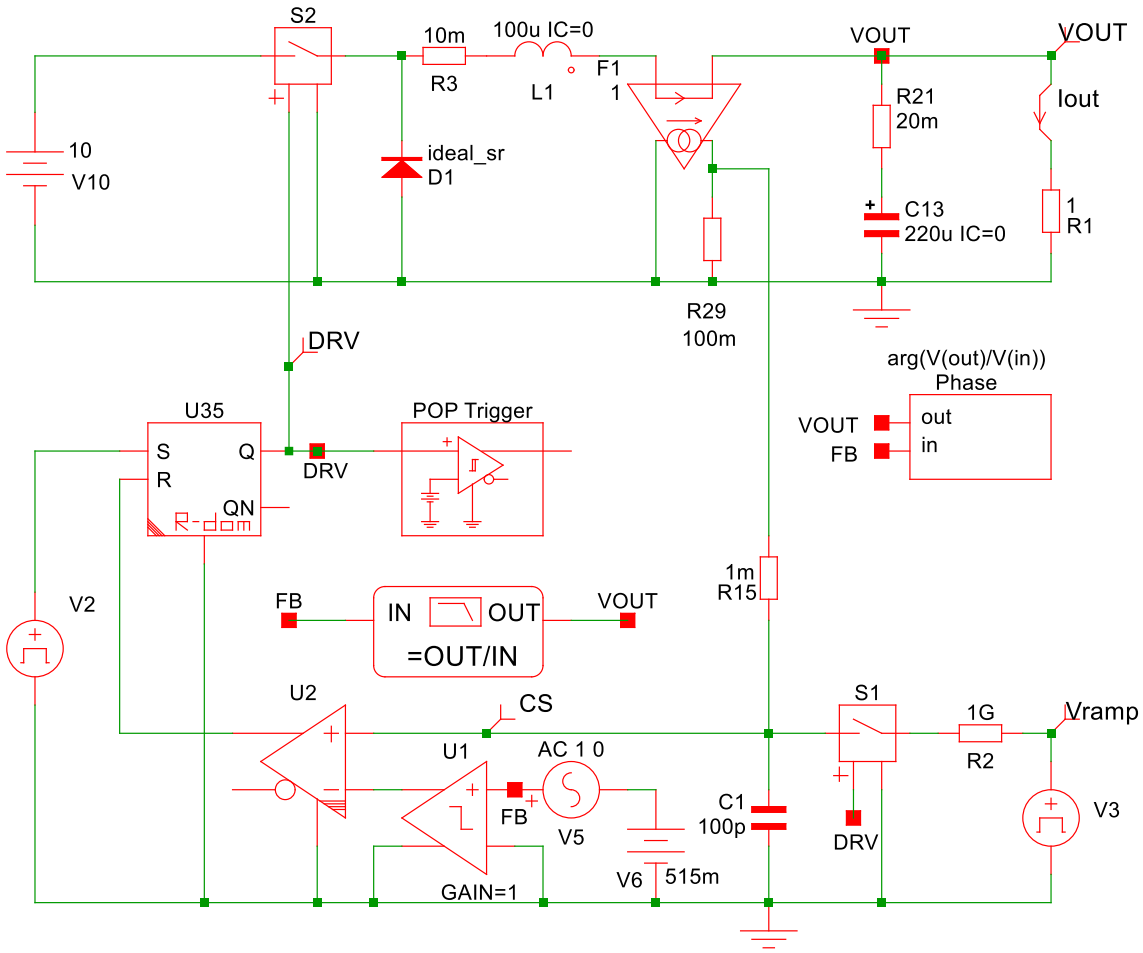
$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{e^{-sT_s}}{1-e^{-sT_s}}$$

Testing the New Implementation

- A single SPICE delay line is associated with an integrator for the current loop
- The rest of the model remains unaffected



$$\frac{e^{-sT_s}}{1-e^{-sT_s}}$$

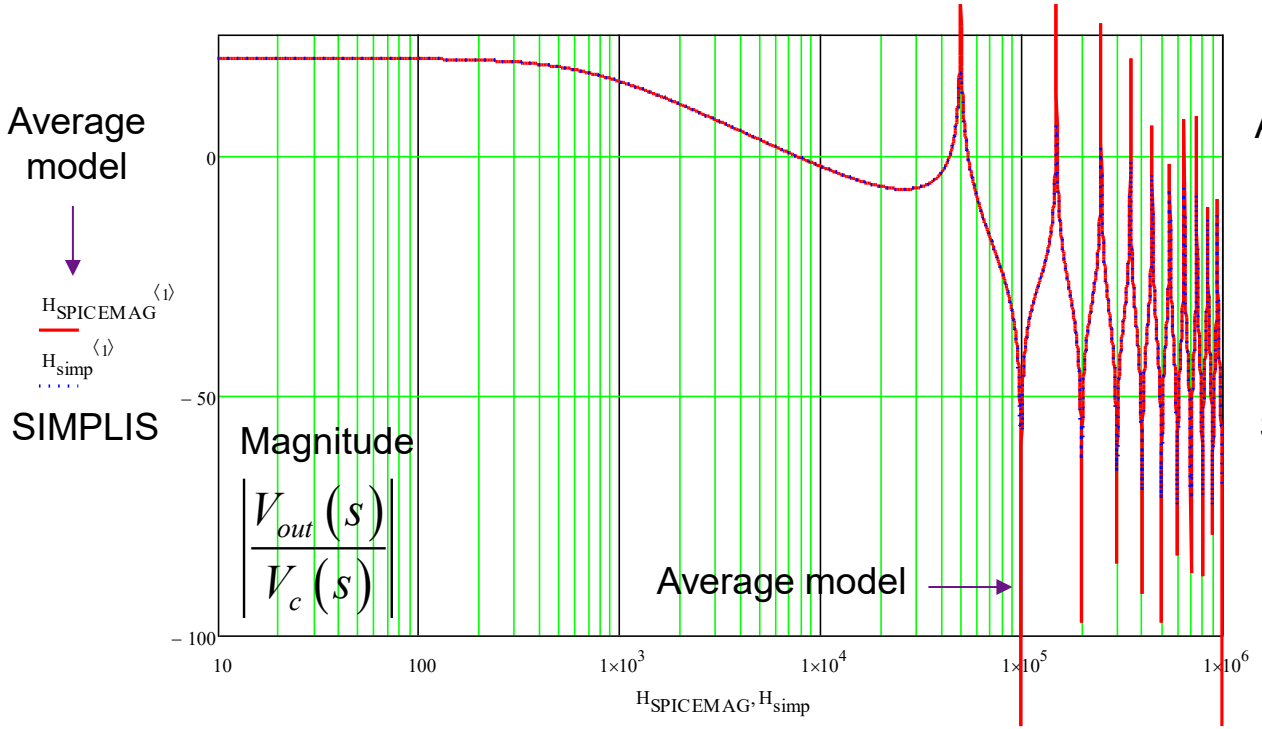


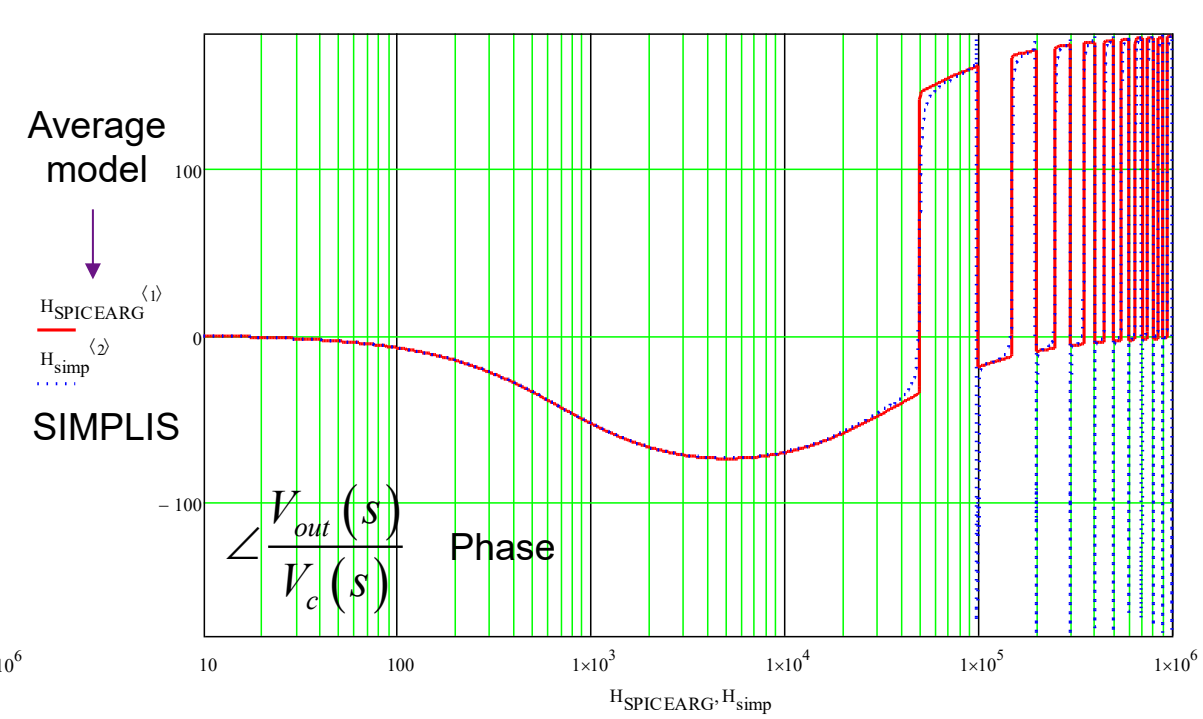
✓ The new block is inserted in the original model

✓ SIMPLIS will give us the small-signal response

Perfect Match between the Circuits

- I have imported the raw data from SPICE and SIMPLIS in a Mathcad sheet
- The correspondence between the two circuits is excellent



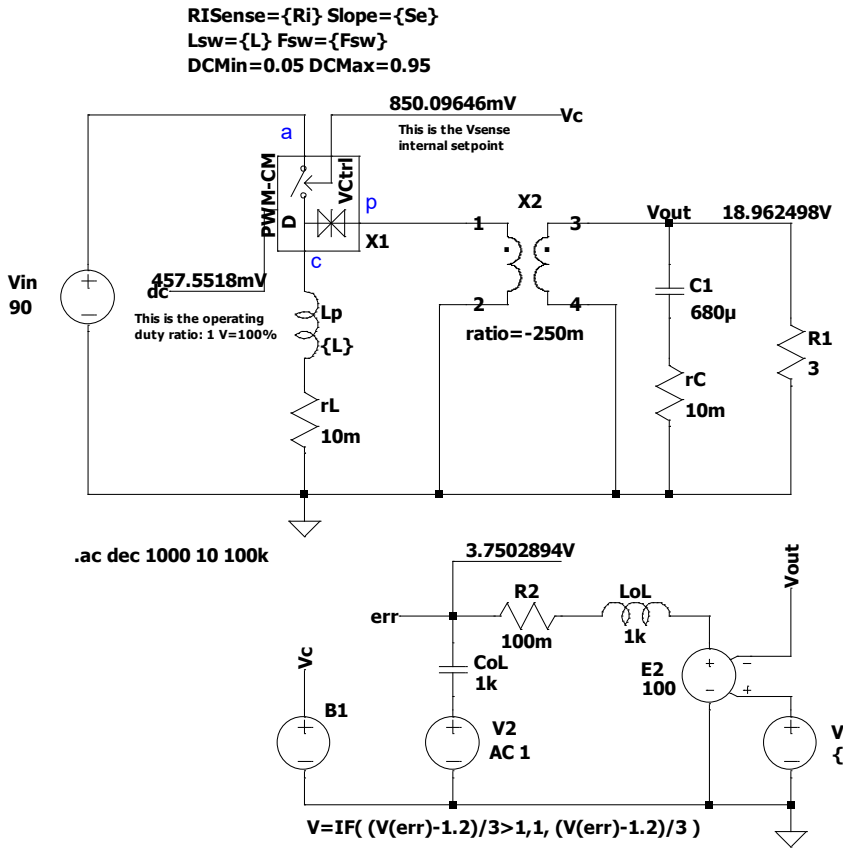


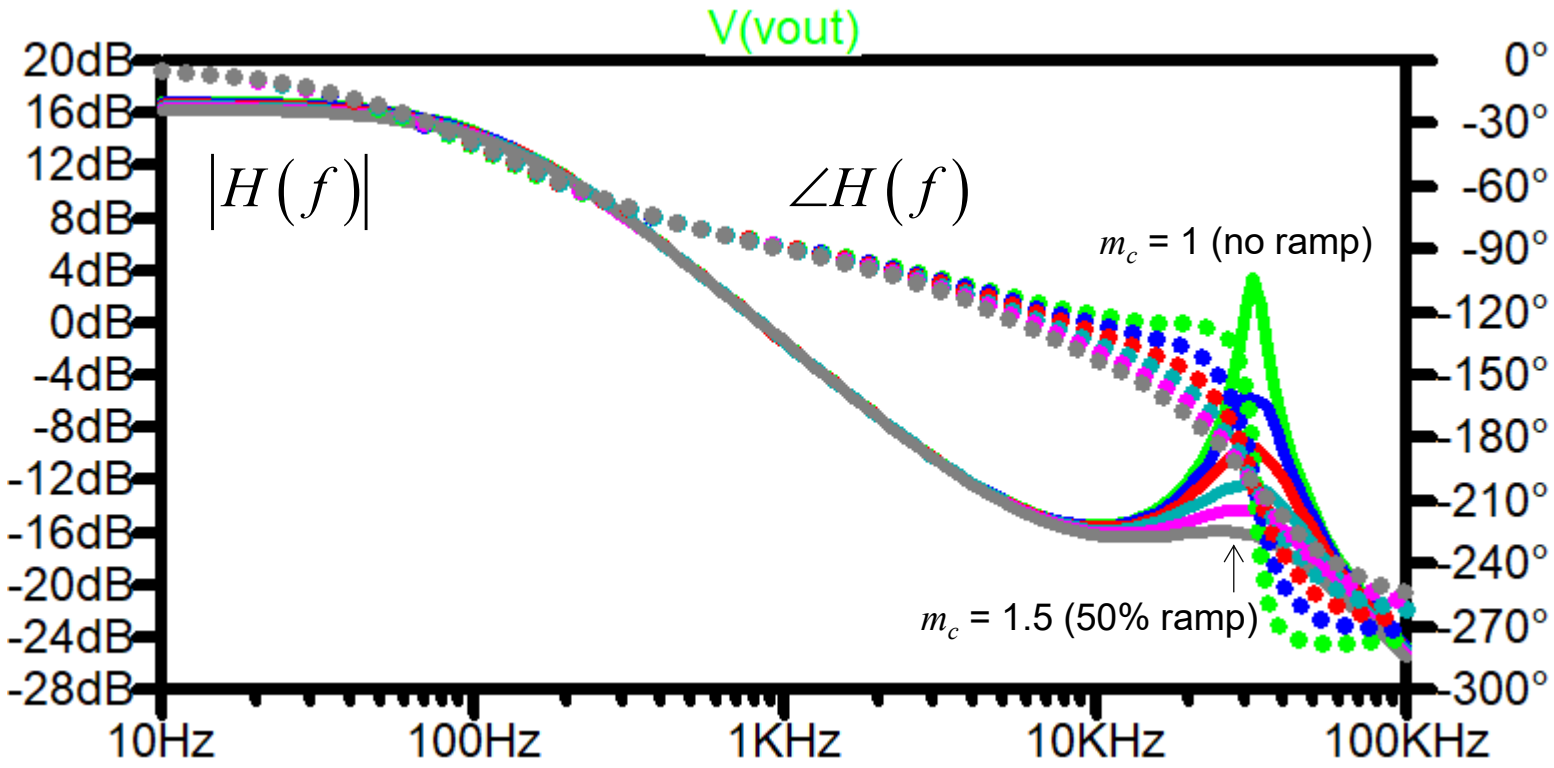
- This approach is helpful to understand the sampled-data model construction
- It however unnecessarily complicates the original model which is SPICE2 compatible

C. Basso, https://powersimtof.com/Downloads/Divers/Ridley%20model.pdf

Visualizing the Subharmonic Peaking

- A flyback converter can be built with the CM PWM switch model
- This subcircuit was published in October 1990 by Vatché Vorpérian
- ✓ It works in .AC and .TRAN analyses and predicts subharmonic oscillations





Agenda

- Theory of operation
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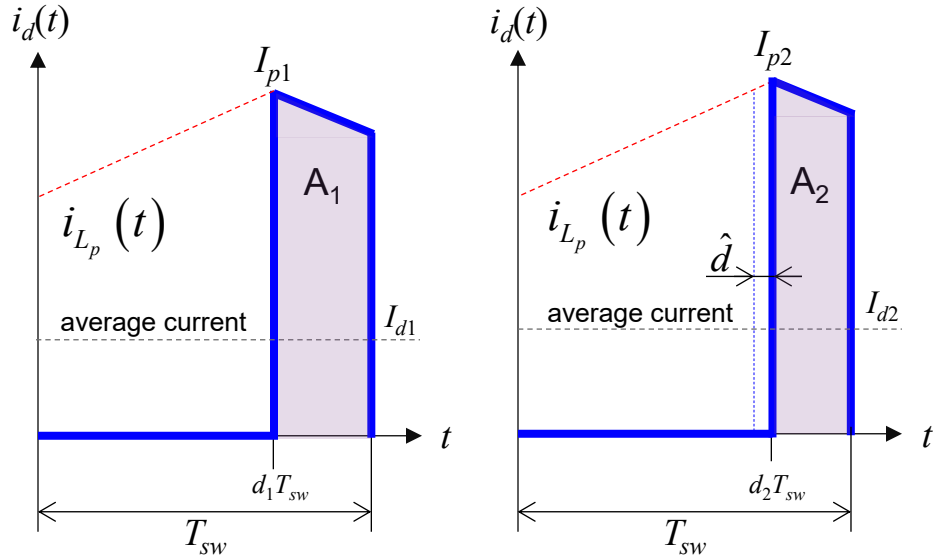
- The Right-Half-Plane Zero
- Closing the Loop with the Flyback Converter

Origins of the Right-Half Plane Zero

- The control-to-output transfer function of the flyback converter includes a RHPZ
- It originates in the two-step store-and-release conversion process
- A small increase in the duty ratio brings a longer output capacitor hold-up time

✓ If the step is too fast, the output voltage first drops before recovering



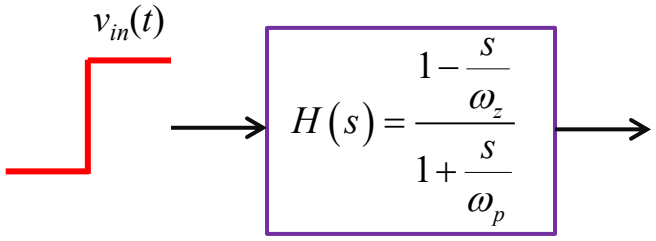
$$I_{out} = \left\langle i_d(t) \right\rangle_{T_{sw}} = I_L(1-D)$$

average

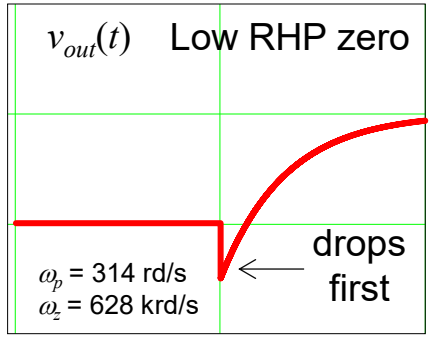
❖ If $I_{p2} > I_{p1}$, then A_2 might be greater than A_1: no V_{out} drop

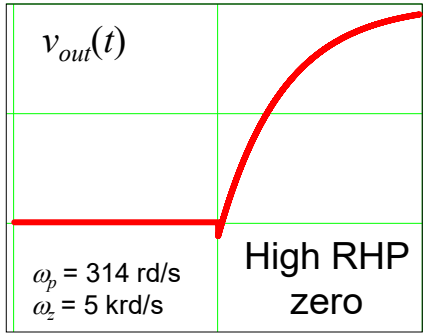
❖ If $I_{p2} < I_{p1}$, then A_2 is smaller than A_1: V_{out} drops!

- The system features a RHP zero
- It is stimulated with a step



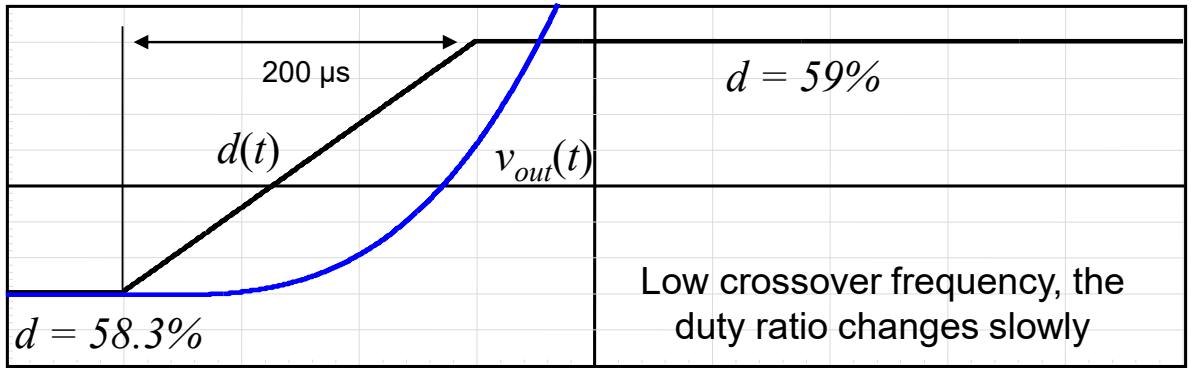
- A low-frequency RHP zero brings an output drop
- Increase the RHP zero frequency or slow-down the step, the drop is reduced

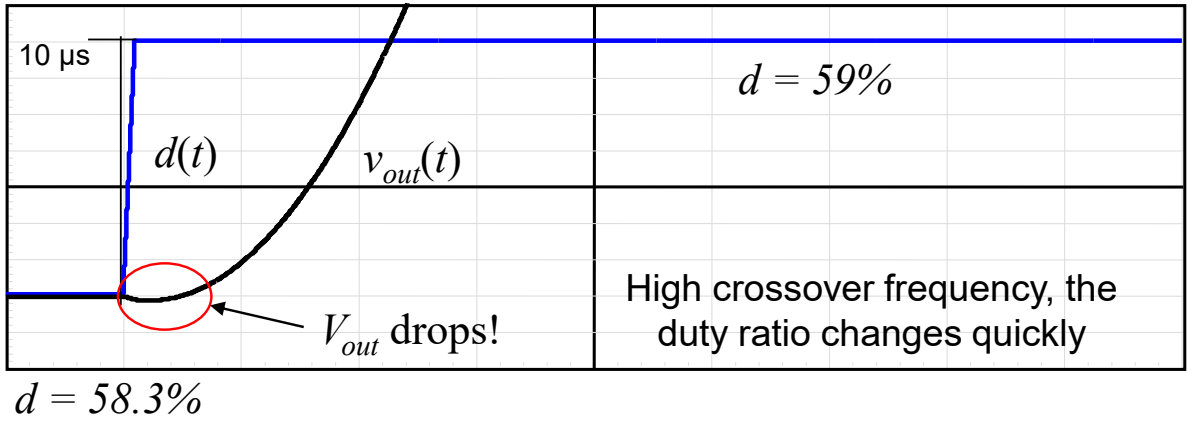


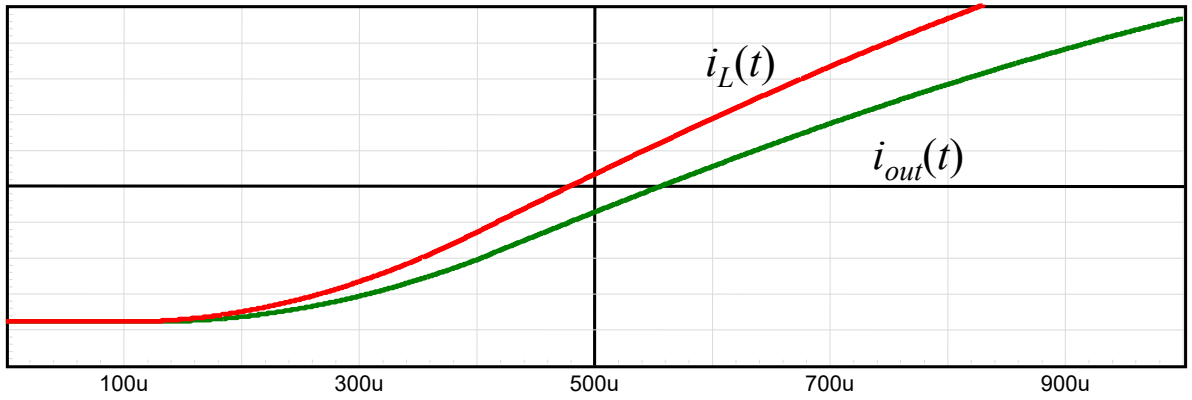


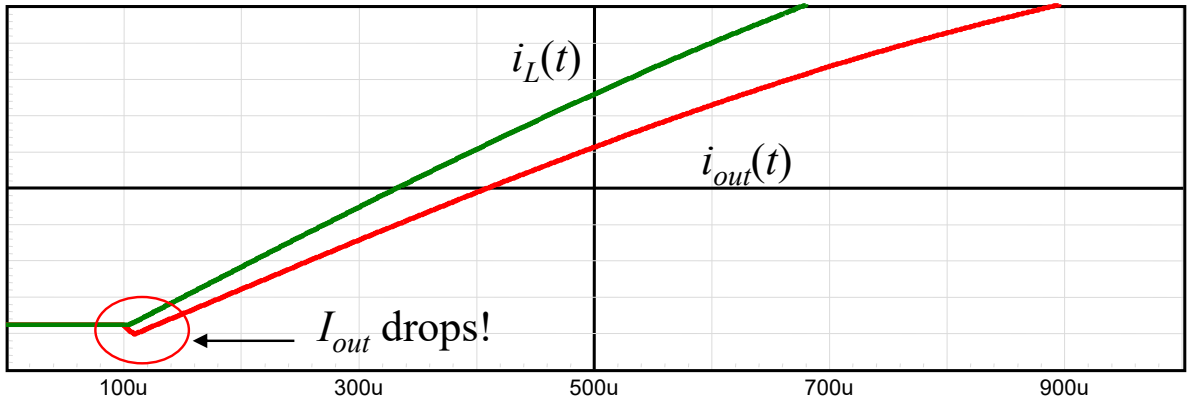
Averaged Model shows the RHPZ Effect

- If the duty ratio is slowly increased – f_c is reduced – there is no drop on V_{out}
- When crossover is extended, the duty ratio varies too fast and V_{out} initially drops









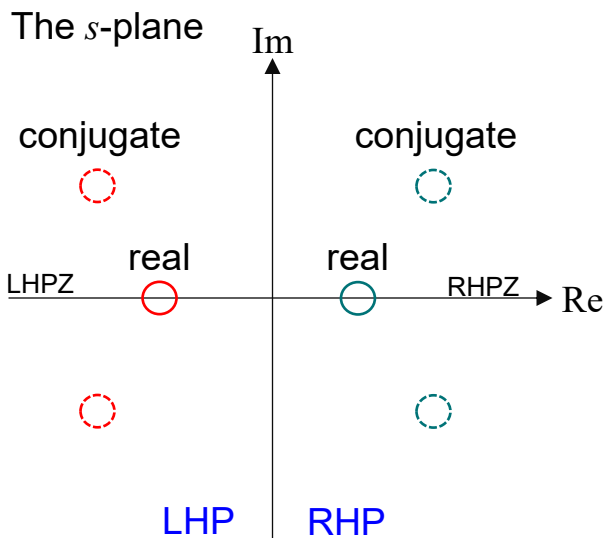
The RHP zero position sets a limits to the maximum allowable crossover frequency

design goal

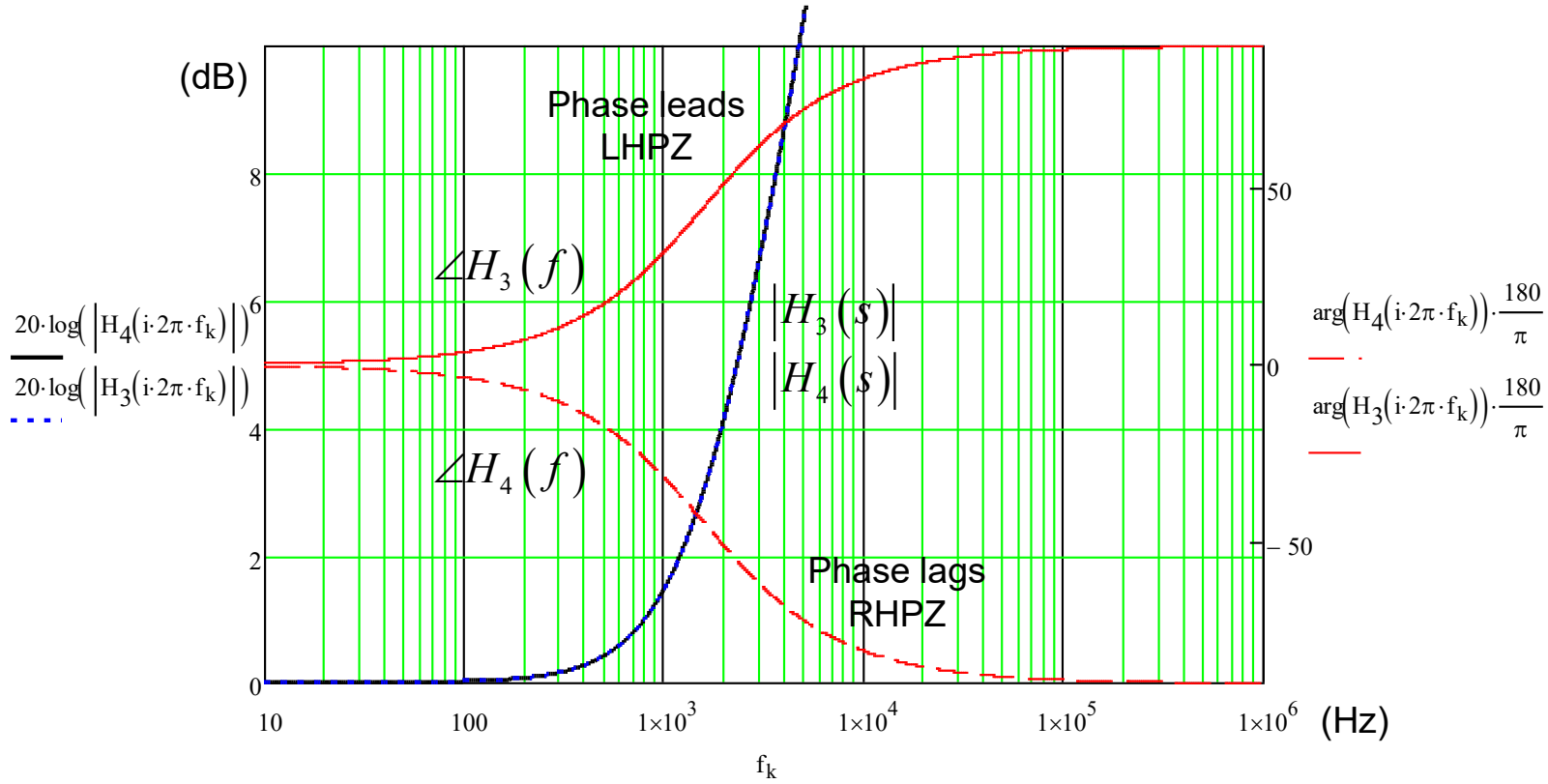
$$f_c < 20\% \; f_{RHPZ}$$

Phase Lag of the Right Half-Plane Zero

- A zero in the left-half-plane – a LHPZ – leads or *boosts* the phase.
- The same zero now lying in the right half-plane – the RHPZ – lags the phase



$$H_3(s) = 1 + \frac{s}{\omega_z} \qquad H_4(s) = 1 - \frac{s}{\omega_z}$$



- The RHP zero phase is reversed compared to that of the LHP zero
  - ❖ This added phase lag may affect the margin at crossover

Control Scheme does not Change RHPZ

- Whether the converter operates in voltage- or current-mode control, RHPZ is there
- It is present in continuous conduction mode and depends on operating conditions
- ✓ Still there in DCM but relegated to higher frequencies owing to a smaller inductance

CCM voltage mode

$$\frac{\hat{v}_{out}(s)}{\hat{d}(s)} = G_0 \frac{\left(1+\frac{s}{\omega_{z_1}}\right)\left(1-\frac{s}{\omega_{z_2}}\right)}{1+\frac{s}{Q\omega_0}+\left(\frac{s}{\omega_0}\right)^2}$$

CCM current mode

$$\frac{\hat{v}_{out}(s)}{\hat{v}_c(s)} = G_0 \frac{\left(1+\frac{s}{\omega_{z_1}}\right)\left(1-\frac{s}{\omega_{z_2}}\right)\left(1+\frac{s}{\omega_{z_3}}\right)}{D(s)}$$

- Before closing the loop, determine the worst-case position of the RHP zero
- ➢ Choose the highest output current and the lowest dc input voltage

$$\omega_{z_2} = \frac{R_{load} D'^2}{N^2 DL}$$

$N_1 := 0.28 \quad V_{in} := 60V \quad D := 41.7\% \quad R_L := 6\Omega \quad L_p := 1mH$

$V_{out} := N_1 \cdot V_{in} \cdot \frac{D}{1-D} = 12.016\,V$

$f_z := \frac{R_L \cdot (1-D)^2}{N_1^2 \cdot D \cdot L_p} \cdot \frac{1}{2 \cdot \pi} = 9.928\,kHz$

$$f_c < 20\% f_z$$

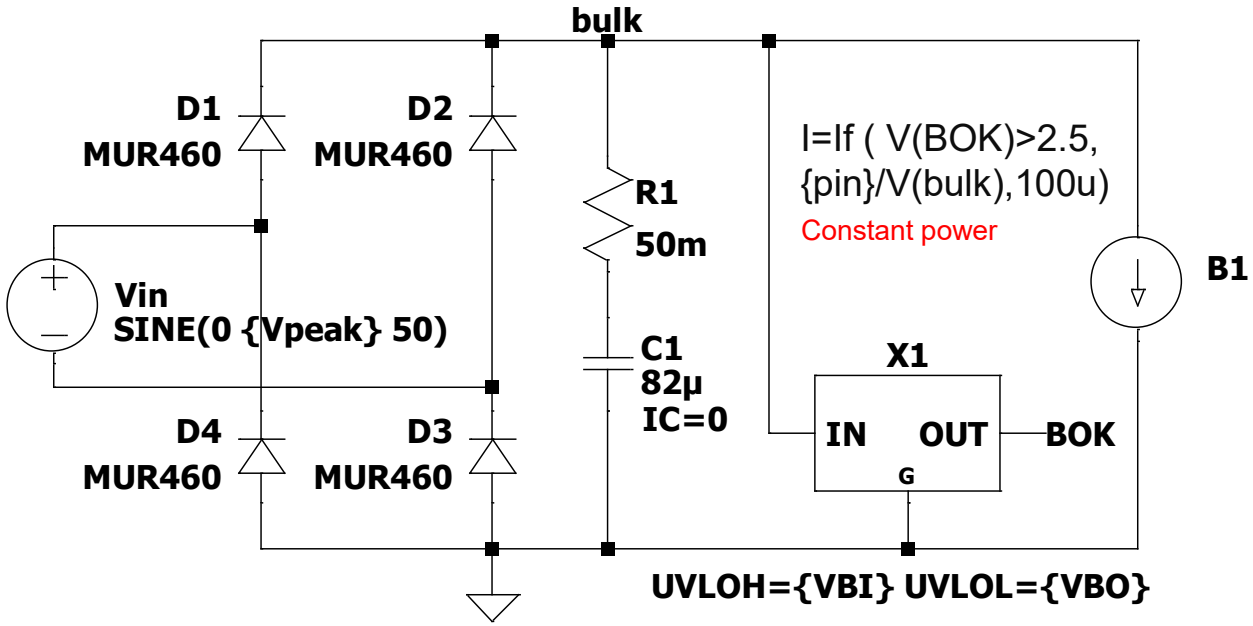
$$f_c < 1.9\ \text{kHz}$$

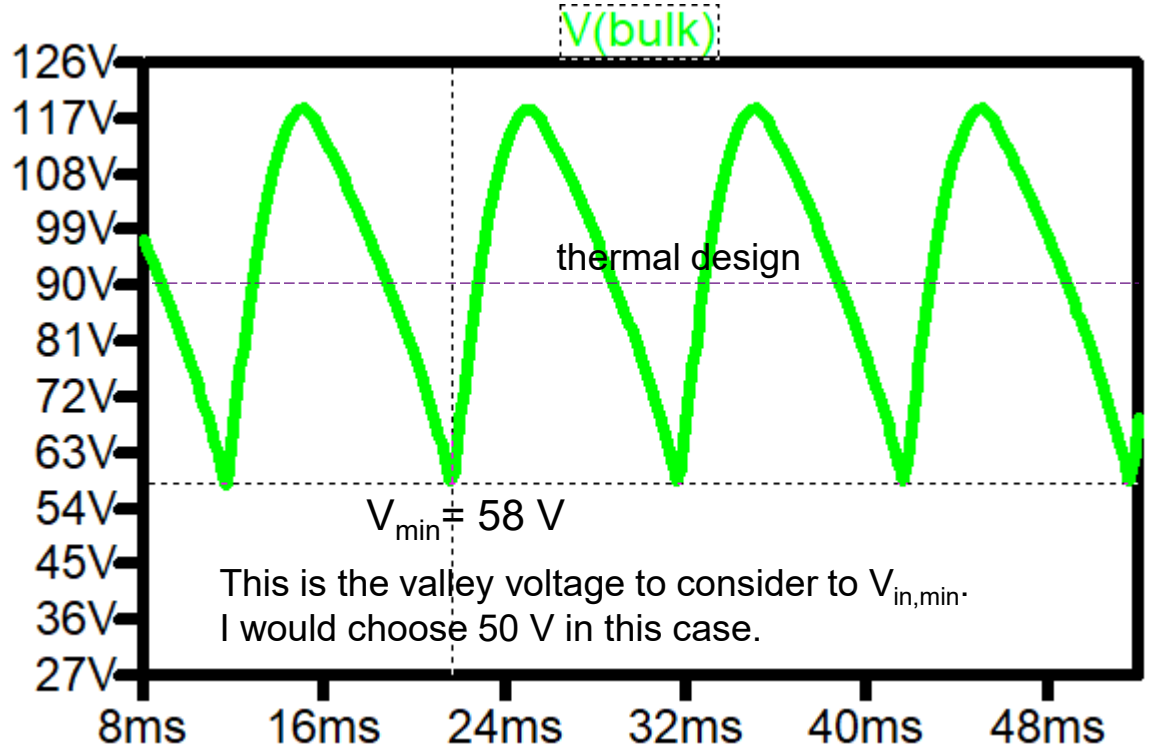
Crossover frequency limit

What is the Lowest Input Voltage in AC?

- The flyback converter is well suited to be supplied from a universal 85-265-V rms input
- The dc input voltage will thus vary between minimum and maximum
- Owing to rectification, the rectified low-line voltage will exhibit peak and valleys

✓ The valley voltage represents the very minimum operating voltage





Agenda

- Theory of operation
- Controlling the Converter
- Current-Mode Instabilities
- The Right-Half-Plane Zero
- Closing the Loop with the Flyback Converter

Closing the Loop of the Flyback Converter

- We assume a 12-V converter delivering 2 A and supplied on universal mains
- You start with the control-to-output transfer function

$$H(s) \approx H_0 \frac{\left(1+\frac{s}{\omega_{z_1}}\right)\left(1-\frac{s}{\omega_{z_2}}\right)}{1+\frac{s}{\omega_{p_1}}} \frac{1}{1+\frac{s}{\omega_n Q_p}+\left(\frac{s}{\omega_n}\right)^2}$$

Sub-harmonic poles

$$H_0 = \frac{R_{load}}{R_{sense} G_{FB} N} \frac{1}{\frac{(1-D)^2}{\tau_L} + 2M + 1}$$

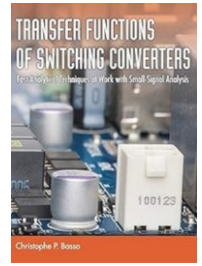
Internal divider in the controller

$$\tau_L = \frac{2 L_p N^2}{R_{load} T_{sw}} \qquad f_{p1} = \frac{\frac{(1-D)^3}{\tau_L} + 1 + D}{2\pi R_{load} C_{out}} \qquad f_{z_1} = \frac{1}{2\pi r_C C_{out}} \qquad f_{z_2} = \frac{(1-D)^2 R_{load}}{2\pi D L_p N^2}$$

This is the RHPZ

$$M = \frac{V_{out}}{N V_{in}} = \frac{12}{0.2 \times 80} = 0.78 \qquad D = \frac{V_{out}}{V_{out} + N V_{in}} = \frac{12}{12 + 0.2 \times 80} = 42.8\%$$

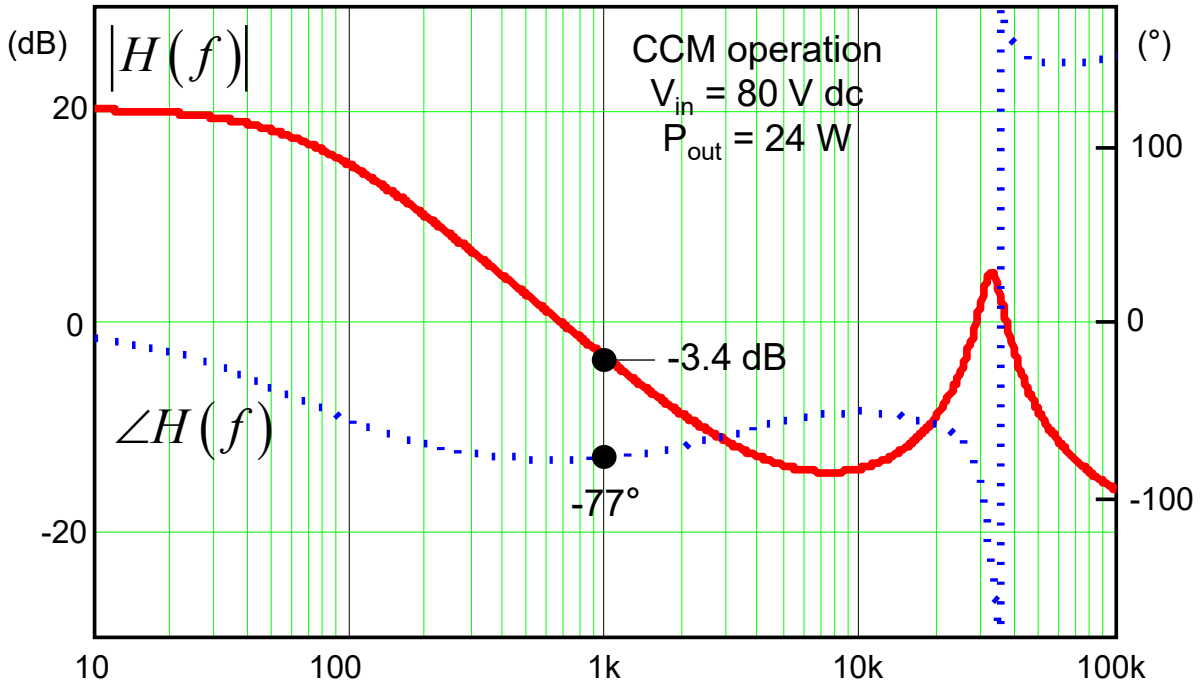
Know the ESR



C. Basso, *Transfer Functions of Switching Converters - Fast Analytical Techniques at Work with Small-Signal Analysis*, Faraday Press, 2021

Extracting the Data at Crossover

- The crossover frequency is limited by the lowest RHP zero position
- Calculations at 80 V dc show a RHPZ located at 17 kHz
- ✓ 20% of this value is 3.4 kHz: the crossover frequency will be 1 kHz



Design parameters:

Converter Parameters Fixed-Frequency Operation

$V_{in\_min} := 80V$ $V_{in\_max} := 370V$ $N_s := 16$ $R_{sense} := 0.33\Omega$ $C_{out} := 680\mu F$

$V_{out} := 12V$ $L_p := 1mH$ $N_p := 80$ $\eta := 85\%$ $R_{esr} := 0.05\Omega$

$P_{out} := 24W$ $V_f := 0.5V$ $N_1 := \frac{N_s}{N_p} = 0.2$ $R_{load} := \frac{V_{out}^2}{P_{out}} = 6\Omega$

Controller Parameters

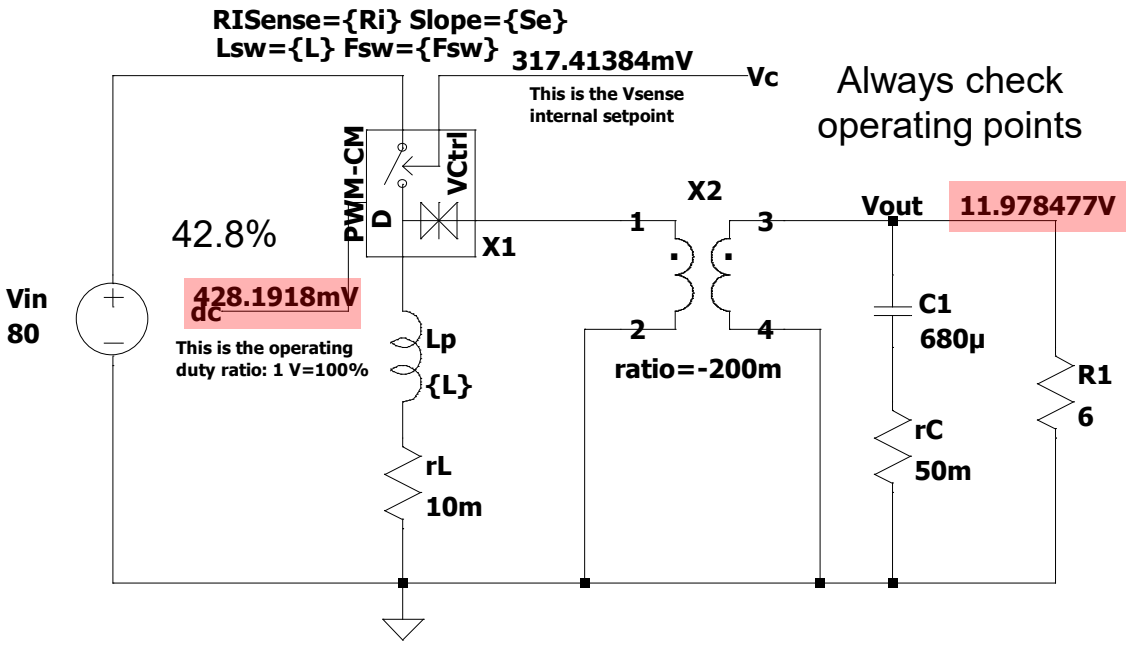
$F_{sw} := 65kHz$ $S_e := 0\frac{kV}{s}$ $Div := 3$ $T_{sw} := \frac{1}{F_{sw}} = 15.385 \cdot \mu s$

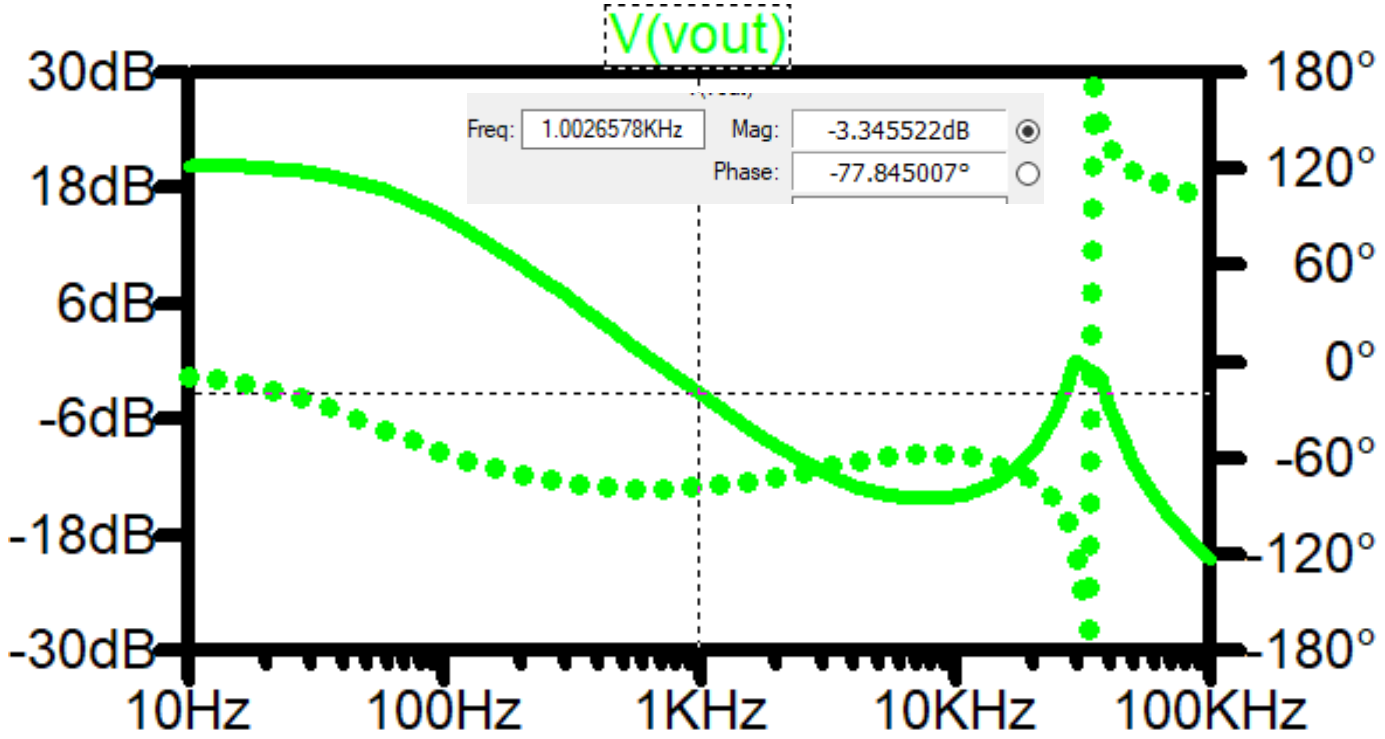
This divider is internal to the IC

- The subharmonic poles are peaking and slope compensation is needed

Validating Data with an Averaged Model

- It is interesting to duplicate the analysis with a SPICE simulation
- The CM PWM switch is well suited to confirm – or not – the validity of the expressions





- The model confirms the calculated operating points with a 42.8% duty ratio

✓ The ac response exactly matches the previous plot

Closing the Loop with a TL431

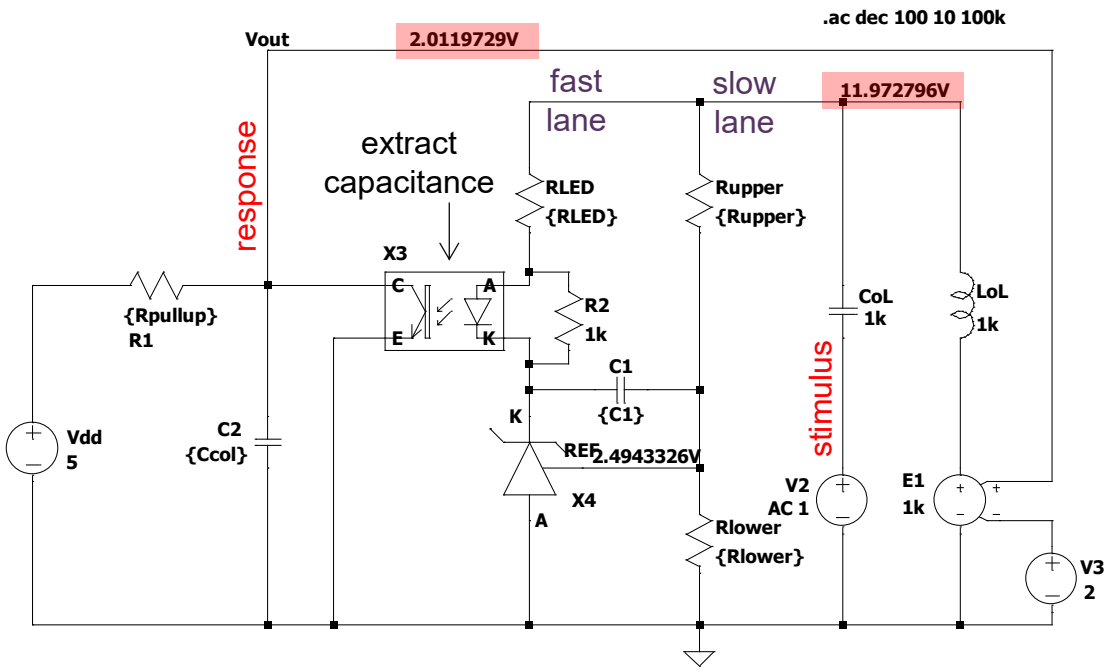
- A type 2 compensator is selected to close the loop with an optocoupler
- The filter combines a pole at the origin and a pole-zero pair

✓ We first shift the magnitude curve by 3.3 dB: $\left|G\left(1\,\text{kHz}\right)\right| = 3.3\,\text{dB}$

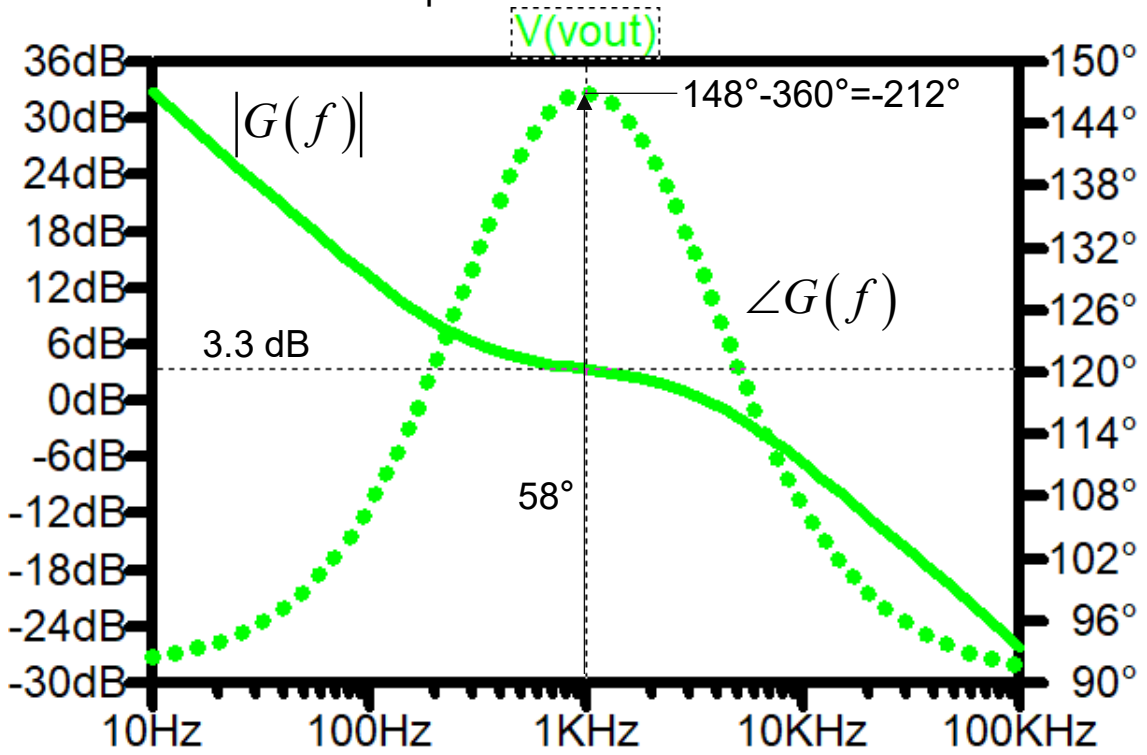
✓ We boost the phase by $\text{PM} - \text{PS} - 90 = 70 + 78 - 90 \approx 58°$ $\longrightarrow \angle G\left(1\,\text{kHz}\right) = -212°$

phase margin target 70°

power stage phase

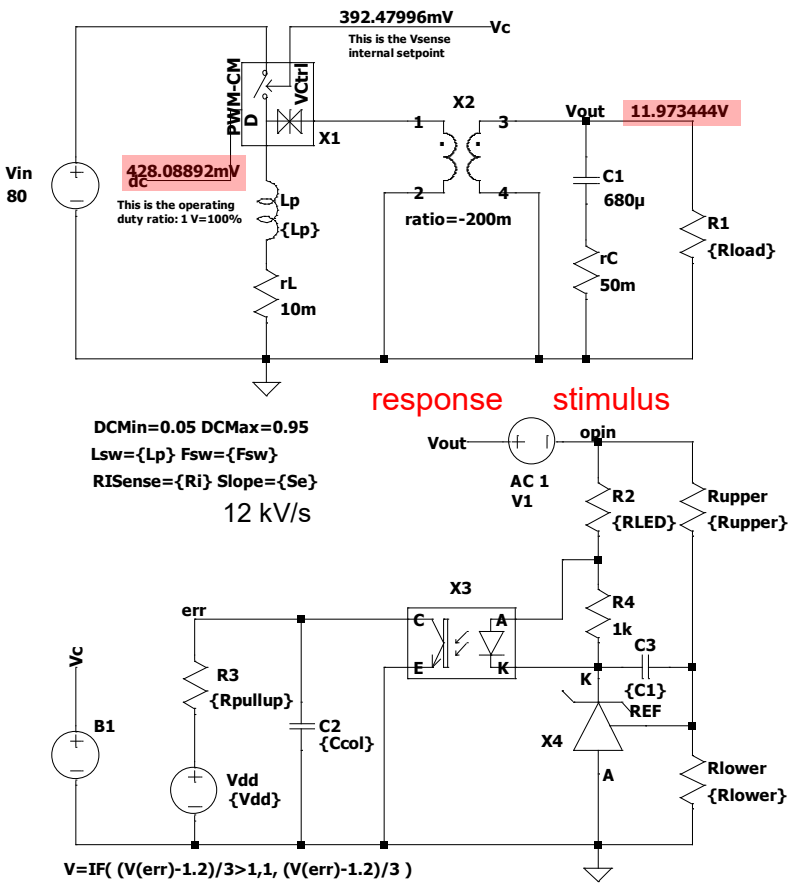


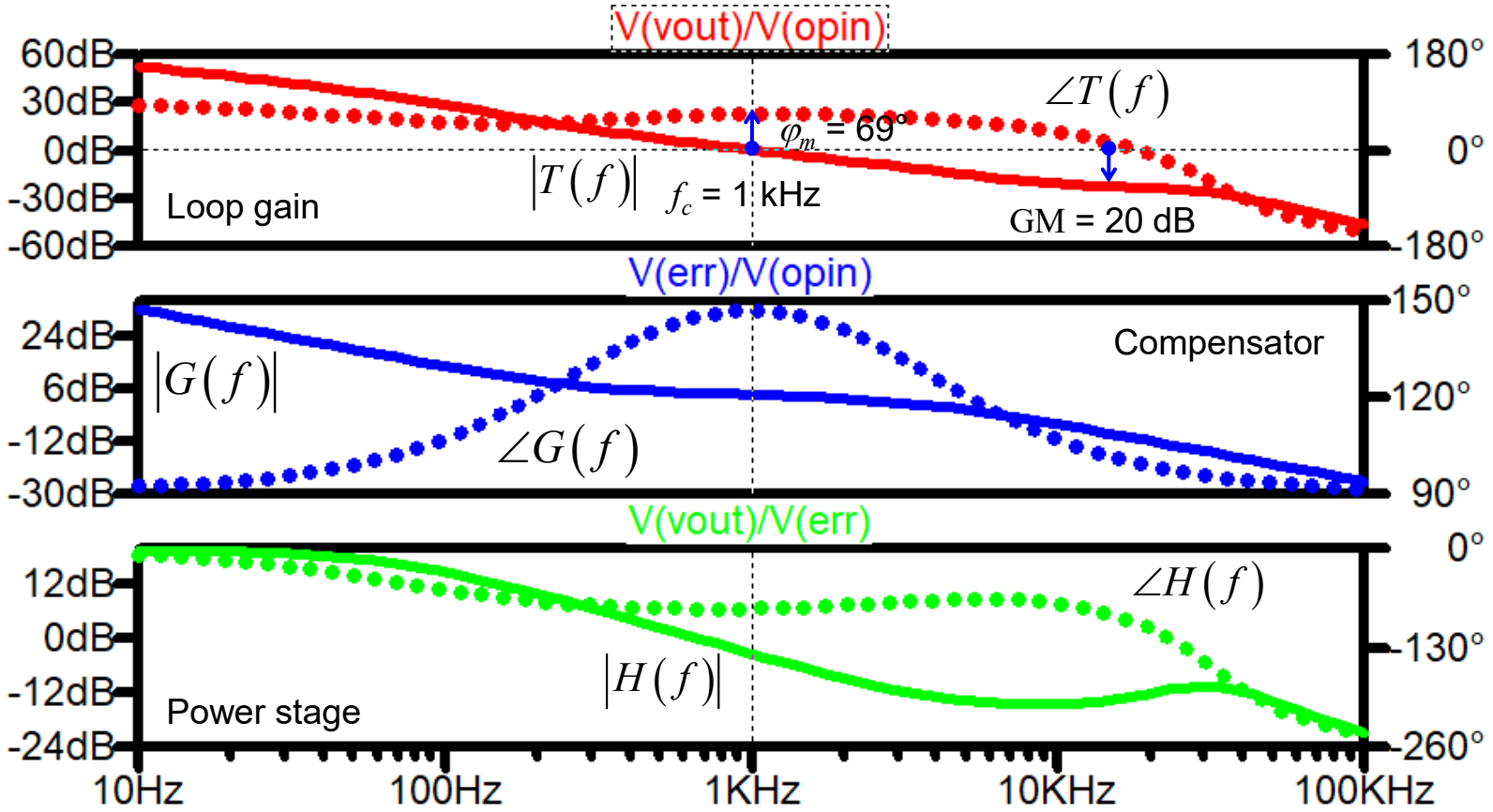
boost in phase



Plotting the Compensated Gain $T(s)$

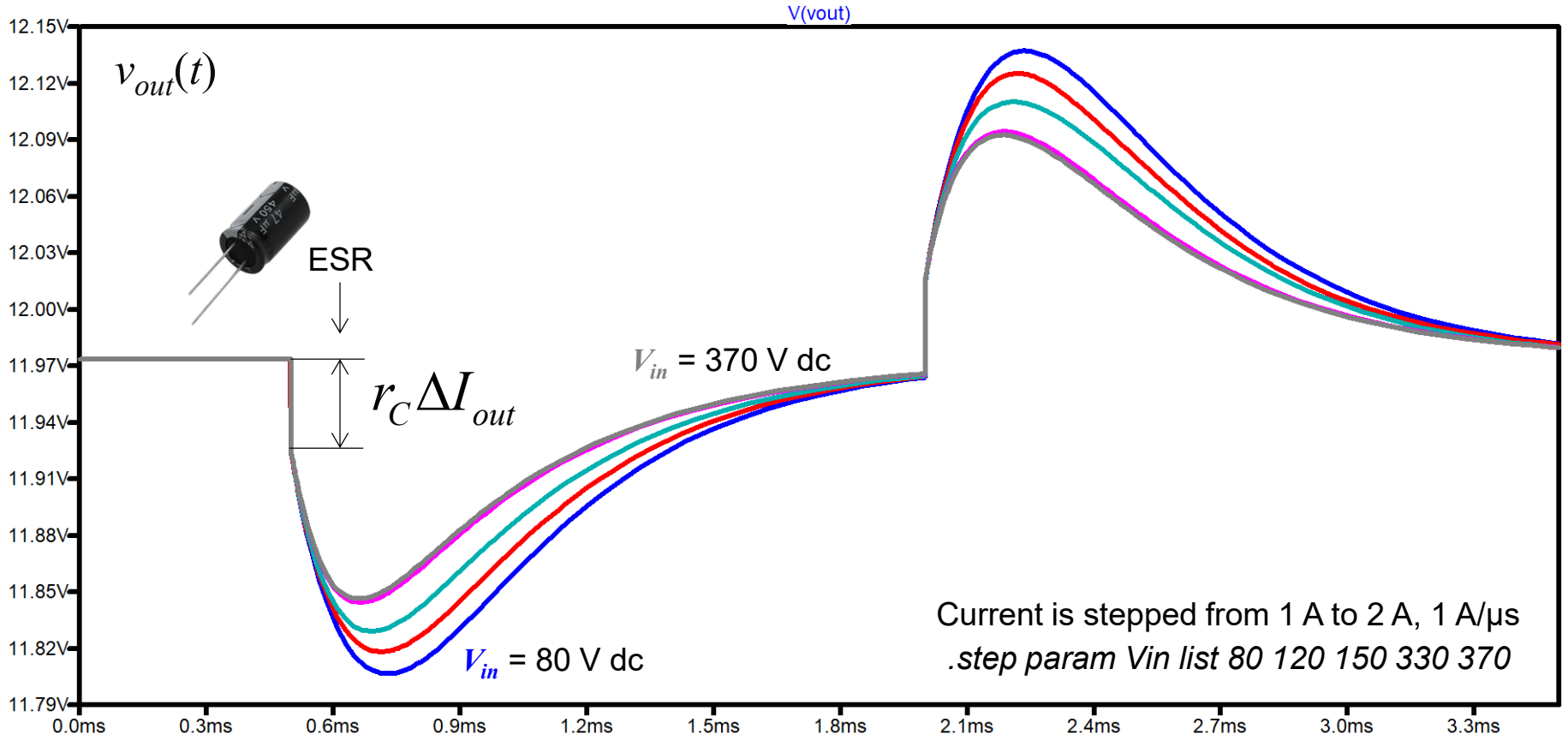
- The compensated loop gain T is made of $T = H(s)$ x $G(s)$
- You have to plot it at different operating points then check crossover and margins
- ✓ Assign tolerances to critical components and run Monte Carlo analyses





Transient Response with Averaged Model

- Nonlinear equations in a large-signal model let you simulate a transient response
- Transient response is interesting to confirm the compensation strategy is adequate
- ✓ Check output voltage undershoots and overshoots in various V_{in}/I_{out} combinations



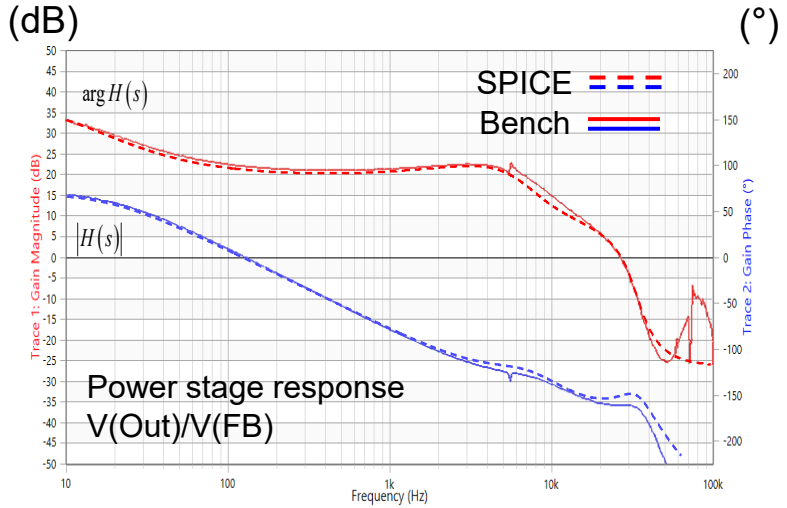
- The input voltage is stepped from 80 V dc (the lowest valley at 85 V rms input) to 370 V dc, which corresponds to the rectified peak of a 265-V rms input voltage.
- The response is very stable with 120-mV undershoots and overshoots.

Measuring the Loop on the Bench

- When the power supply is stabilized, you must check it stability on the prototype
- The first step requires a frequency-response analyzer or FRA

✓ You need to connect the fast- and slow-lanes together for injection

Injection transformer



- Use PCB test points to connect the probes and the ac source
- Make sure these points and injection resistance R_5 (10-20 Ω) are included during design phase

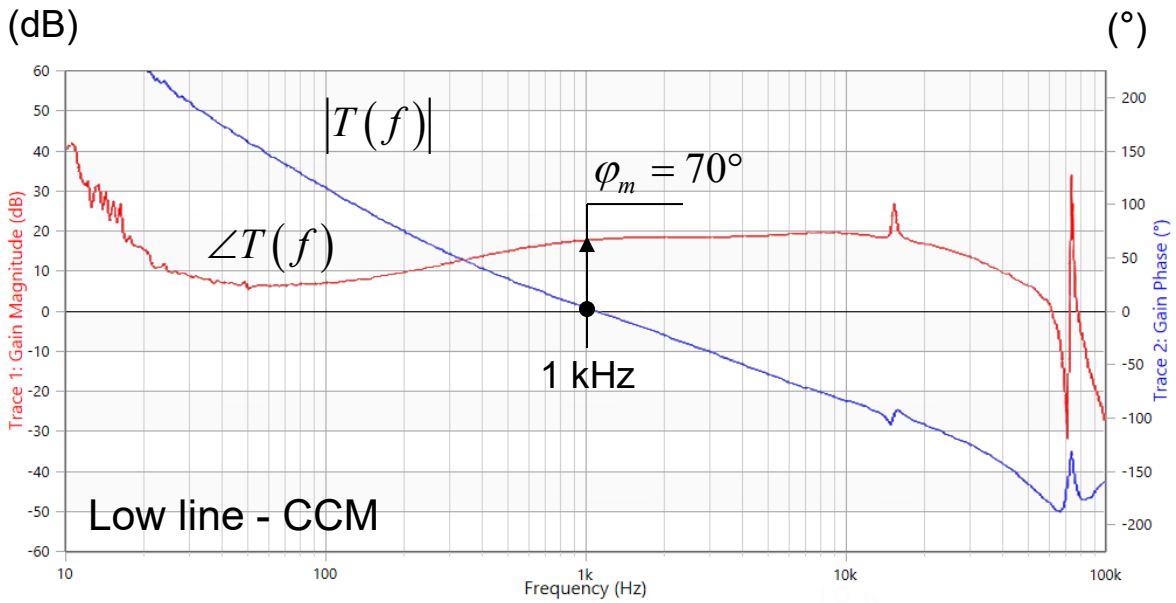
❖ You don't want to cut traces on a multi-layer PCB to inject the modulation

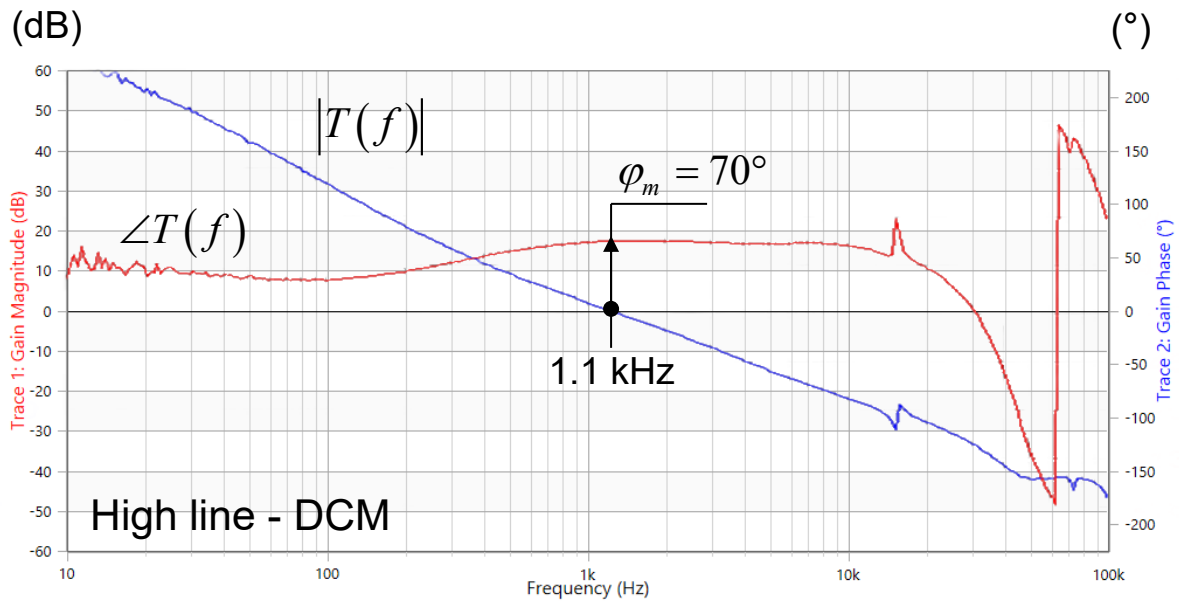
- With a TL431 configuration, sweep the two lanes at once or apply superposition
- The bench measurement has two purposes:

✓ Validate your compensation strategy
✓ Tweak the model to reflect the measurement
➢ It leads to a simulation circuit you can trust

Compensated Loop Measurements

- It is an essential part of stability and reliability assessment, you cannot skip it
- Step-load response is important also but does not provide any margin information
- ✓ Parasitics move with production and lifetime: check you always have margins!

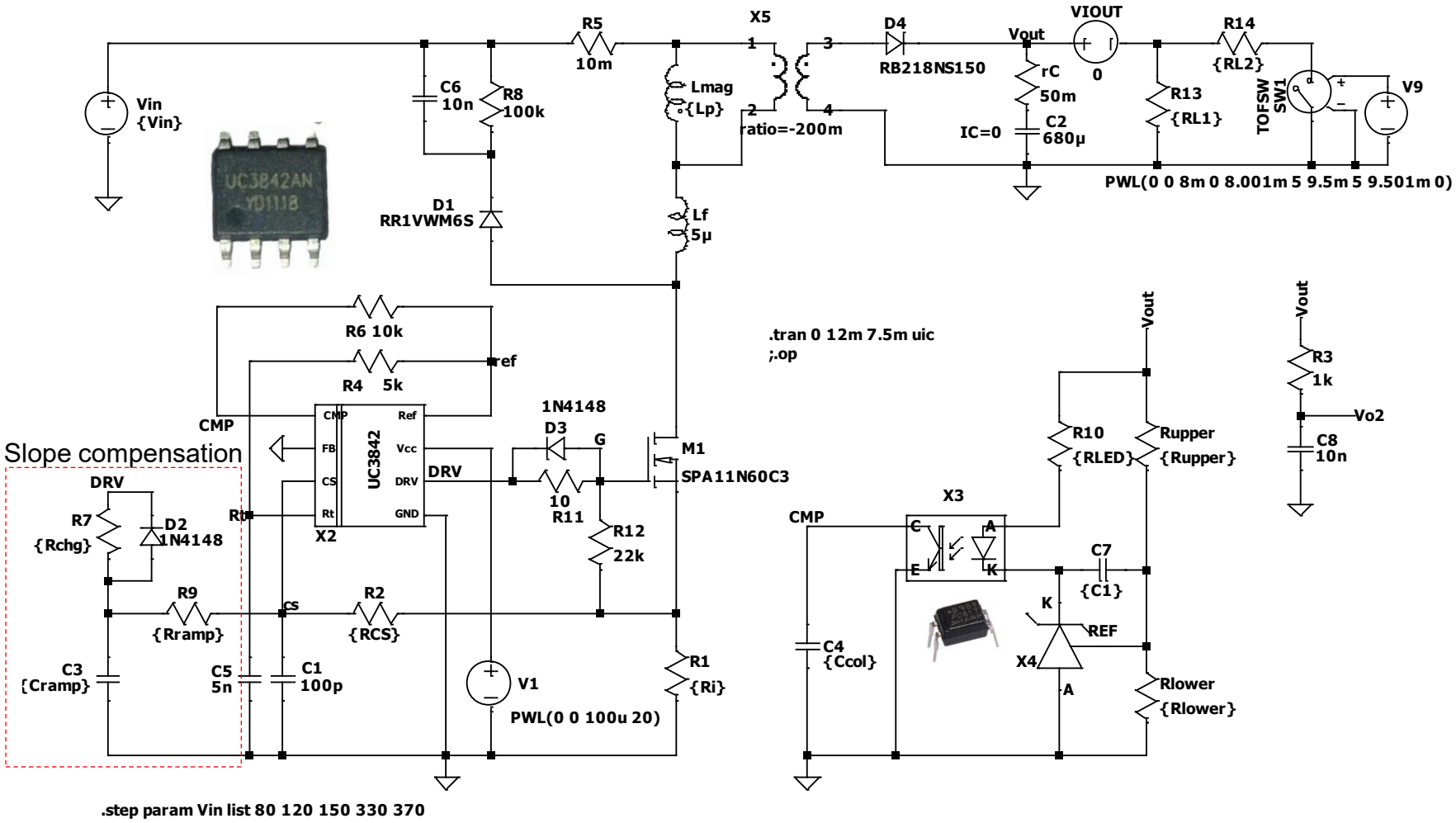




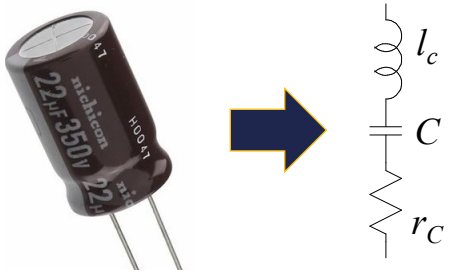
- Reduce the modulation amplitude as the ac source approaches the crossover frequency
- Owing to current-mode control, the transition from CCM to DCM is smooth

The Complete Cycle-by-Cycle Model

- The cycle-by-cycle model uses a classical UC3842 controller
- Capacitors and the transformer include their parasitics: leakage and ESR



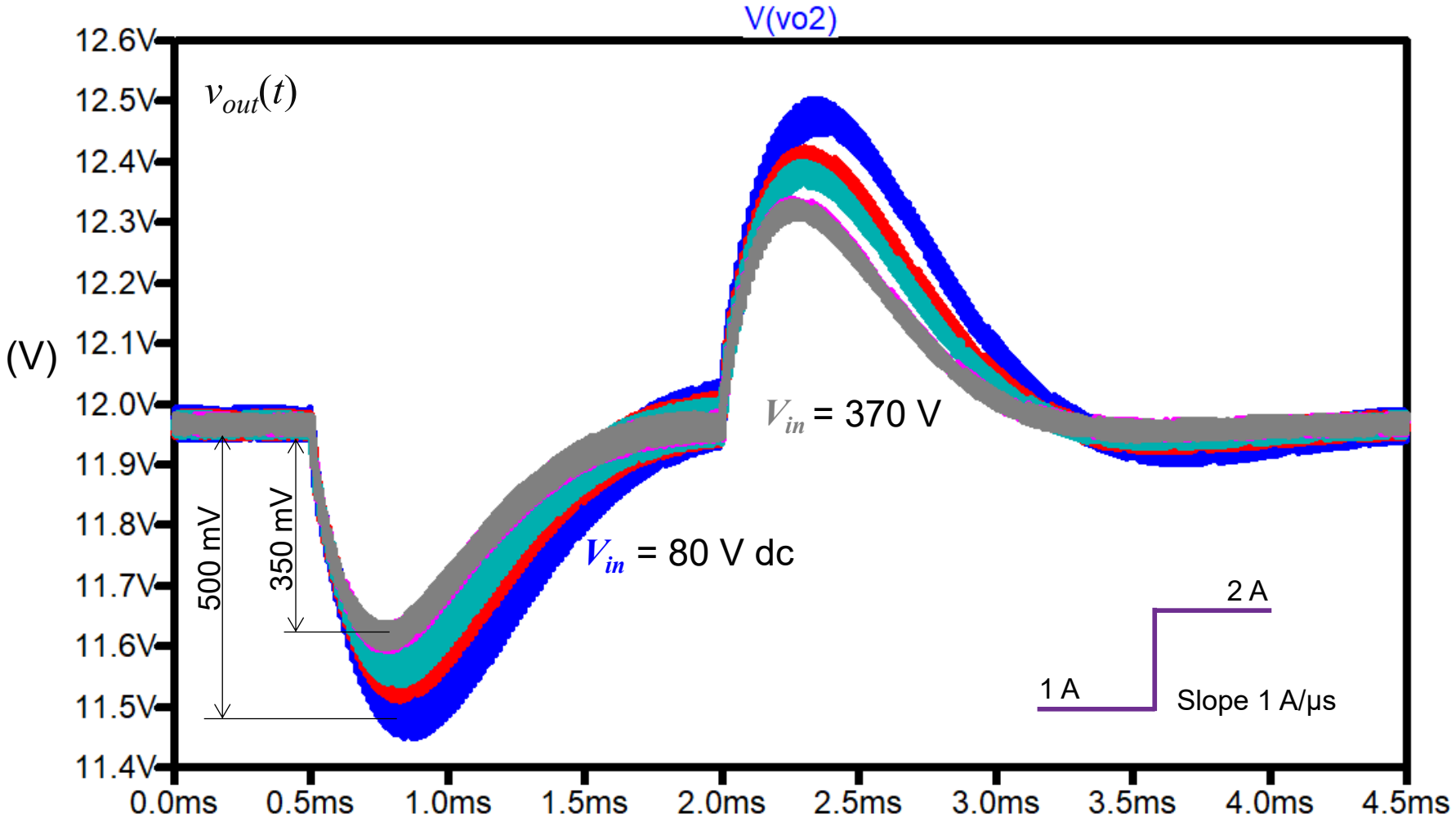
- Extracting the component parasitics is key to obtaining good results
- These offenders are the transformer leakage inductance, the output capacitor ESR – noted r_C



- Do not forget the optocoupler for which you need its collector-emitter parasitic capacitor

Transient Responses in Low and High Line

- The current is stepped from 1 to 2 A at two different input voltages
- The response is very stable at both extremes with less than 4% undershoot at 80 V dc



- The first drop is due to the output capacitor ESR
- The undershoot depends on C_{out} and the crossover frequency.
- The recovery time is linked to the phase margin, around 70° here.

Conclusion

- The flyback converter is one of the most popular structures in consumer markets
- It is important to realize how parasitics can impact the performance of the converter
- ✓ The leakage inductance plays a damping role and affects the dc transfer characteristic
- ✓ It defeats cross-regulation performance in multi-output power supplies
- In current-mode control, subharmonic oscillations are coming from the current loop
- ✓ A pair of RHP zeros in the current loop turn into a pair of subharmonic poles at $F_{sw}/2$
- The right-half-plane zero defeats speed and forces a limit to the crossover frequency
- ✓ Determine its position at the very minimum input voltage, the bulk valley level in ac-dc
- Always measure the loop on the bench!

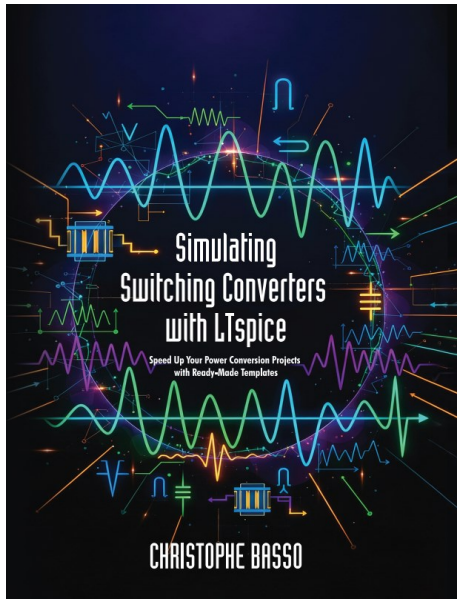
I'm done, merci, thank you!

Snowshoeing is way cooler than flyback design!

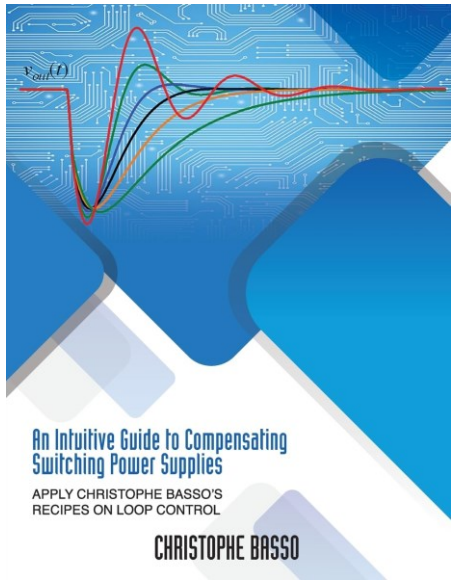
https://powersimtof.com/Spice.htm

Models and Additional Reading

- The LTspice/SIMPLIS models can be downloaded from my webpage: https://powersimtof.com/Spice.htm
- J. Picard, Under the Hood of Flyback SMPS Designs, SEM1900, Texas-Instruments
- I. Cohen, B. Keogh, Flyback Transformer Design Considerations for Efficiency and EMI, Design Seminar 2016/2017, Texas-Instruments (PPT version)



How to use my 200+ ready-made switching templates



If you want a crash course on loop control, this book is for you!

If the weather is rainy for 1 month or so, why not try small-signal analysis?